DOCUMENTATIE
P. 2000

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1 GENERAL DESCRIPTION

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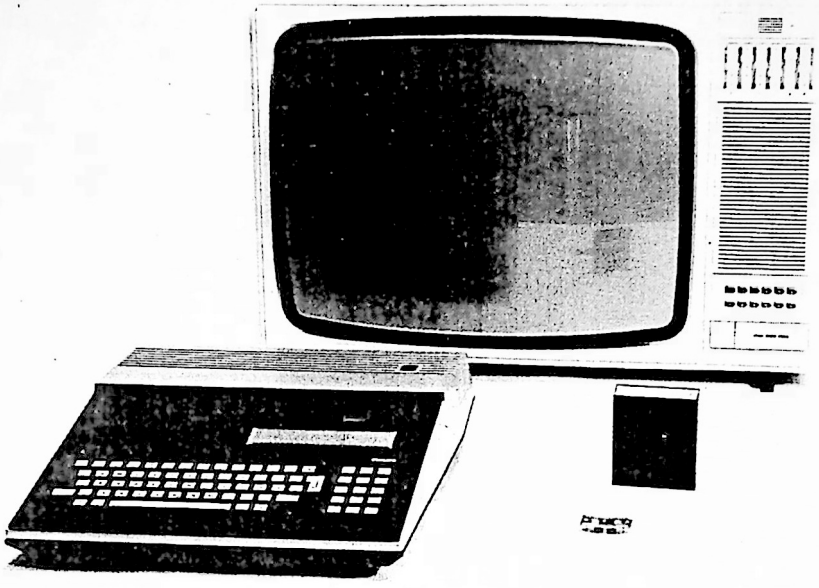

Figure 1.1 P2000 T-VERSION

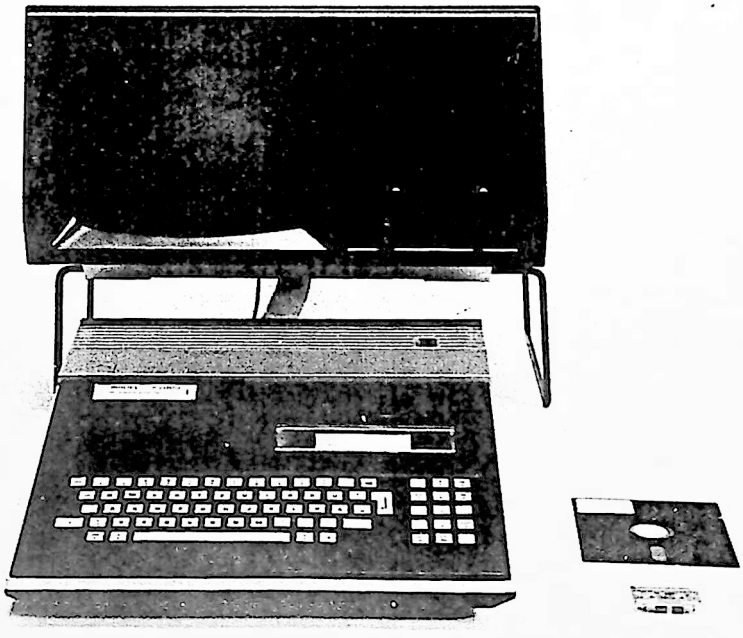

Figure 1.2 P2000 M-VERSION

1.1 SYSTEM INTRODUCTION

The P2000 Microcomputer is available in two versions:

- T-version
- M-version

The T-version consists of one cabinet, the basic cabinet (figure 1.1). This computer interfaces to either a standard black/white or colour television set or a special set with non-modulated R.G.B interface.
The basic cabinet includes a keyboard and minicassette drive and is equipped with a serial printer interface.
Standard programs are available on ROM-cartridges which can be plugged into a slot on the cabinet.
A second slot is available for installation of an optional interface adaptor, for example a modem-interface.

The M-version consists of two cabinets, the basic cabinet and the monitor cabinet (figure 1.2).
The basic cabinet includes the same functions as the T-version, but interfaces to a professional monitor in the monitor cabinet.
This monitor cabinet is also the housing for upto 2 mini floppy disk drives.

This manual is intended to give support information about the functional and detailed operation of the P2000 Microcomputer, both for M- and T-version.
Not included in this manual is a description of the internal and external peripherals.
For this information we refer to the particular service manuals. Field Service information of the computer is given in the P2000 Field Service Manual.

2 FUNCTIONAL DESCRIPTION

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2.1 INTRODUCTION

The P2000 is a microcomputer system consisting of the next four functional groups:

- CPU
- Memories
- I/O control
- Video Generation

The main difference between the T- and M-version of the P2000 is found in the video generation. The T-version interfaces to a standard black/white or colour televisionset and is controlled by logic circuitry on the CPU-board.
The M-version interfaces to a professional 12" monitor and is controlled by logic circuitry on a separate video board.
For both versions the extension board is optional.

2.2 CPU

The CPU is a Zilog Z80 microprocessor.
The µ-processor offers a 16 bit addressbus and an 8 bit databus.
Instructions are fetched via the databus. The instruction set includes a wide variety of instructions such as logical and arithmetic operations, jump and move instructions, a set of memory load and store commands and I/O instructions.
During memory operations the address bus carries the specific memory address.
During I/O operations the address bus carries the specific portnumber which is involved.
The selection of the particular memory area and the selection of a particular I/O port is done by decoding a part of the addressbus.

2.3 MEMORIES

The CPU is addressing a number of memory areas, each of them with a specific function.
The MONITOR ROM is a 4K8 (4096x8) read only memory. This ROM contains the general routines to operate the machine.
It includes a start-routine which is accessed after POWER-ON and initializes the machine (memory test, initialization of I/O controllers, screen initialization, etc.).
Furtheron the MONITOR ROM contains the general I/O routines to control the hardware such as a keyboard scan routine (every 20 ms on interrupt base), a printer-routine including serializing and error control, cassette interfacing including motor control, error check and serializing, a routine to activate the BELL, and a bootstrap routine for the mini floppy system.

The APPLICATION PROGRAM is stored on ROM's in the PROGRAM CARTRIDGE. This cartridge is inserted onto the CPU-board via a slot on the machine. Various programs are available such as wordprocessing, basic, etc.
The program memory can go upto 16K8.
It is started after the machine is initialized by the monitor.
It includes the specific routines for an application.
For access to the hardware at certain points the program makes use of the monitor routines, for example to read a record from tape, to print a line on the printer or to display information on the video screen.

The system RAM is a random access read-write memory consisting out of 8 dynamic memory chips of 16K1.
Part of the system RAM is reserved for the communication between the application program and the monitor routines.

It includes several flags about the configuration of the machine, keyboard buffer, status octads, stack-area etc.
The other part of the system RAM is free for the application program, program variables, databuffers, etc.

The video memory is different for the T- and M-version.

For the T-version this memory is a 2K8 area to be loaded with the information to be displayed. It includes the control characters of the teletex characterset, while also cursor information is stored in the memory. 1920 locations are used to enable the display of 40 characters in 24 rows on the TV-screen and the scrolling of 40 characters on every row.

For the M-version this memory consists of 2 areas. An area of 2K8 is used to store the 1920 characters to be displayed on the screen (80 characters, 24 rows). Another area of 2K4 is used to store the additional information of the characters to be displayed, such as underline, blinking, graphic and inverse video (attributes).

The character and attribute information is mixed together for display on the screen and can be considered then as a 2K12 memory for display.
The video memory is addressed by the CPU to store data into the memory and read it by the CPU. The other addressing of the video memory is used for screen refresh, which requires a fetch of characters to be displayed on regular moments to the video generation logic.

Two more memory banks are located on the extension board. Each bank is a 16K8 area, formed out of 8 dynamic memory calls of 16K1 each.
The memory extension can be used by the application to extend the storage area of the system.
The upper 8K of this extension is not directly accessable and is especially used in disc systems to store part of the operating system.

2.4 I/O CONTROL

The CPU controls input and output via a number of I/O ports.
These I/O ports vary from a simple flip-flop, e.g. controlling the BELL, to an intelligent programmable controller circuit, e.g. the FLOPPY-CONTROLLER.
The addressbus, carrying the portnumber during I/O operations of the CPU, is decoded to select the particular I/O port. Data and commands are then offered via the databus.

The keyboard is scanned every 20 ms for key suppression and via an input port the information of the suppressed key is then fetched by the CPU.
The system software is taking care for the translation into a correct value according to the national version and stores the keycode in a buffer area of the system RAM.

The cassette and printer interface is also achieved via a port circuitry, controlled by routines in the monitor program. A second slot is available on the machine to insert an I/O cartridge. This allows a user to adapt other peripherals to the machine with help of an interface circuitry mounted on the I/O cartridge (e.g. viewdata, parallel printer).

The control of the mini floppy disk drives is realized with help of an interface circuitry based on an intelligent floppy disk controller circuit.
Data transfers between floppy and CPU are performed by CPU-scanning of the floppy controller.

Service requests and failure reports are executed on an interrupt base, using the interrupt controller.
The interrupt controller is formed by a programmable counter/timer circuit providing interrupt addresses for floppy and keyboard. It provides also the transmission timing for the optional data communication interface.

When the extension board is not used the keyboard interrupts are generated via a circuitry on the CPU-board giving every 20ms an interrupt to scan the key matrix.

2.5 VIDEO GENERATION

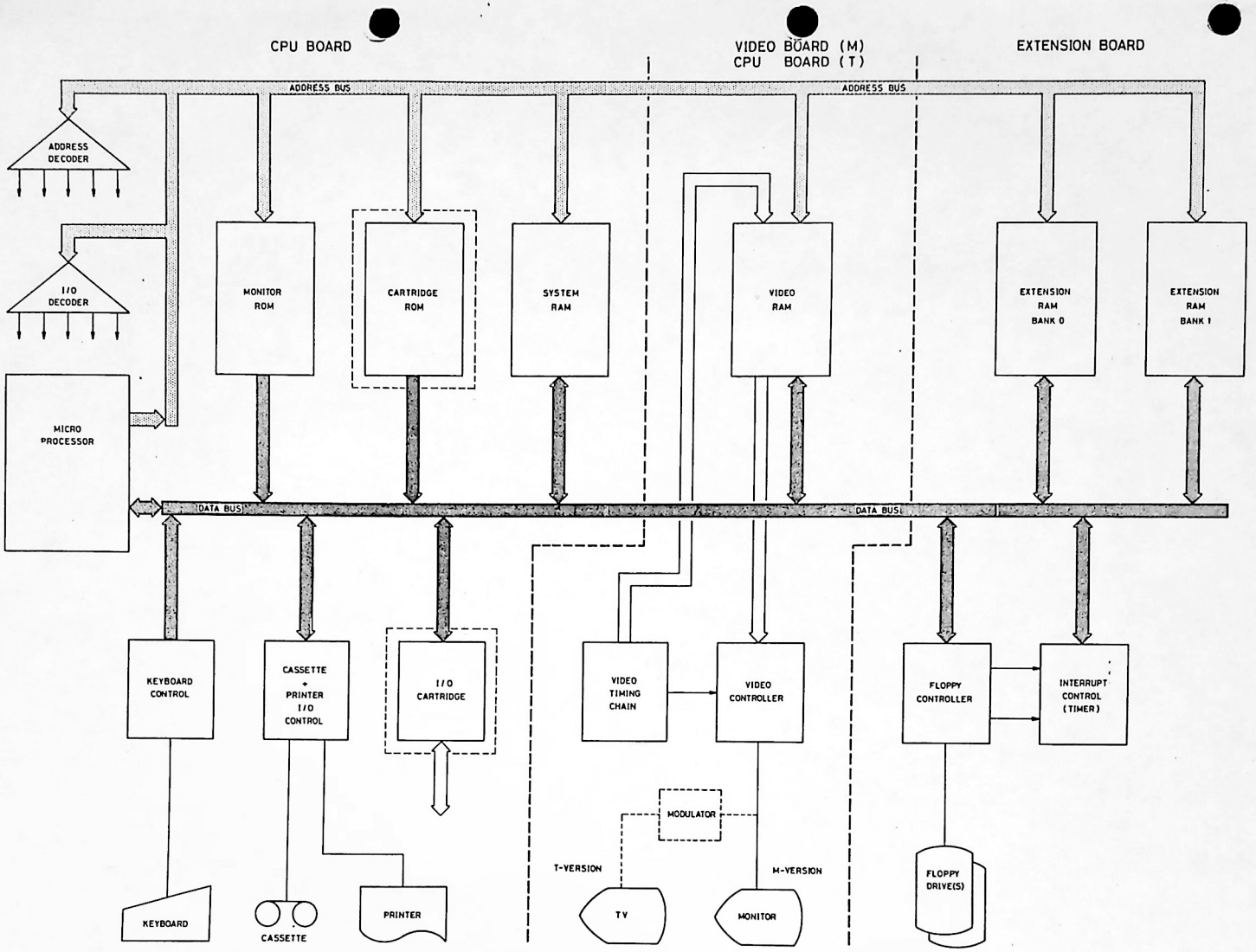
2.5.1 T-VERSION

On the T-version the logic circuitry for video generation is part of the CPU-board.
The circuitry offers two interfaces, one for the connection to the antenne input of a standard television set, a HF modulated signal. The other interface is provided for connection to a televisionset with RGB interface, which is directly giving the red, green and blue levels, thus improving the quality of the green picture.

The screen is refreshed by regular access to the VIDEO RAM. The memory is accessed in this display mode via DMA (direct memory access), the address being offered by the video timing chain.
The data is then fetched to a video generation circuit to translate the coded characters to a serial video dot pattern and decode the special control characters (e.g. COLOUR-SETTING).
The video RAM for the T-version is an area of 2K8, structured as 24 rows of 80 characters each. Only 40 characters of every row are displayed, selected via a scrolling feature under software control.

2.5.2 M-VERSION

For the M-version the video generation is situated on a separate board, called the video board.
It interfaces to a professional video monitor offering a screen of 24 rows of 80 characters.
The display of special features such as blinking characters, inverse video and underlining of characters, is separately controlled per character.
This requires a separate video memory for attributes. Thus the total video memory is formed by a 2K8 memory for characters and a 2K4 memory for attributes.
During screen refresh the video information is extracted both from the character and the attribute memory, offering 12 information bits to the video generation logic. Reading out of the video memory to the video generation logic is not controlled by the CPU but is achieved via a DMA-process, activated and addressed by the video timing chain.



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3.1 CPU-BOARD (FIGURE 4.4)

The CPU-board is split into four functional sections. The first two sections are common for T and M-versions, the last two sections are only used in the T-version.

- CPU/Memory (T + M)
- I/O control (T + M)
- Video Memory (T)
- Video Generation (T)

3.1.1 CPU/MEMORY (FIGURE 4.6.1)

The SYSTEM TIMING is formed by a 20 MHz crystal clock and a divider circuit. The circuitry provides a 2.5 MHz timing signal for the microprocessor (Ø), a 5 MHz timing signal to be used for memory timing (Ø2) and a 4 MHz signal used for the floppy controller on the extension board (T4M).
The microprocessor is a Z-80 CPU circuit. The 16 bits adressbus (A0-15) is providing the selection of I/O ports and addresses the memory locations.
Data transfers are made via the 8 bit bidirectional databus (D0-7).
A number of control signals are offered by the µ-processor to indicate the kind of transfer and data direction according to the next table.

CONTROL SIGNALS	ADDRESSBUS	DATABUS
MREQ, RD, M1	A0-15 Memory address	Instruction fetch
MREQ, RD	A0-15 Memory address	Memory read
MREQ, WR	A0-15 Memory address	Memory write
MREQ, RFRSH	A0-6 Memory refresh address	-
IOREQ, RD	A0-7 Port address	Input from port
IOREQ, WR	A0-7 port address	Output to port
IOREQ, M1	-	Read interrupt vector

The ADDRESS DECODER is decoding the five most significant address lines (A11-15) and offers the chip selection signals for the several memory areas including a memory bus enable signal for the memories connected via a busdriver. The decoding is performed as follows:

ADDRESS LINE 15 14 13 12 11	SELECTION signals	MEMORY AREA
0 0 0 0 0	ROMS1, MBEN	Monitor ROM: 0000 H-0FFF H
0 0 0 0 1	ROMS2, MBEN	
0 0 0 1 X	CARS1, MBEN	ROM Cartridge: 1000 H-4FFF H
0 0 1 0 X	CARS1, MBEN	
0 0 1 1 X	CARS2, MBEN	
0 1 0 0 X	CARS2, MBEN	
0 1 0 1 0	VIDS	Video RAM(T): 5000 H-57FF H
0 1 1 X X	RAMS1, MBEN	System RAM: 6000 H-9FFF H
1 0 0 X X	RAMS1, MBEN	
1 X 1 X X	RAMS2	Extension: A000 H-FFFF H RAM

The MEMORY TIMING is providing the necessary timing for the system RAM (figure 3.1). These RAM circuits are using multiplied addressing. The address is offered in two stages, first the row address (A0-6) and then the column address (A7-13). The memory timing offers the signal SCA to select either row address or column address to be offered to the memory.

Strobing of the row address is done first at MREQ (MRQ) and strobing of the column address is achieved with signal CAS. This signal is generated one clock-pulse time after MRQ and appears only if the system RAM is selected (RAMS1) and no refresh is active (RFRSH).
Refreshing of the dynamic memory cells is achieved with a RAS-only cycle, the row address being offered by the CPU, sequentially refreshing all 128 rows in the memory chip within 2ms.
The signal RFSH appears once per instruction cycle.

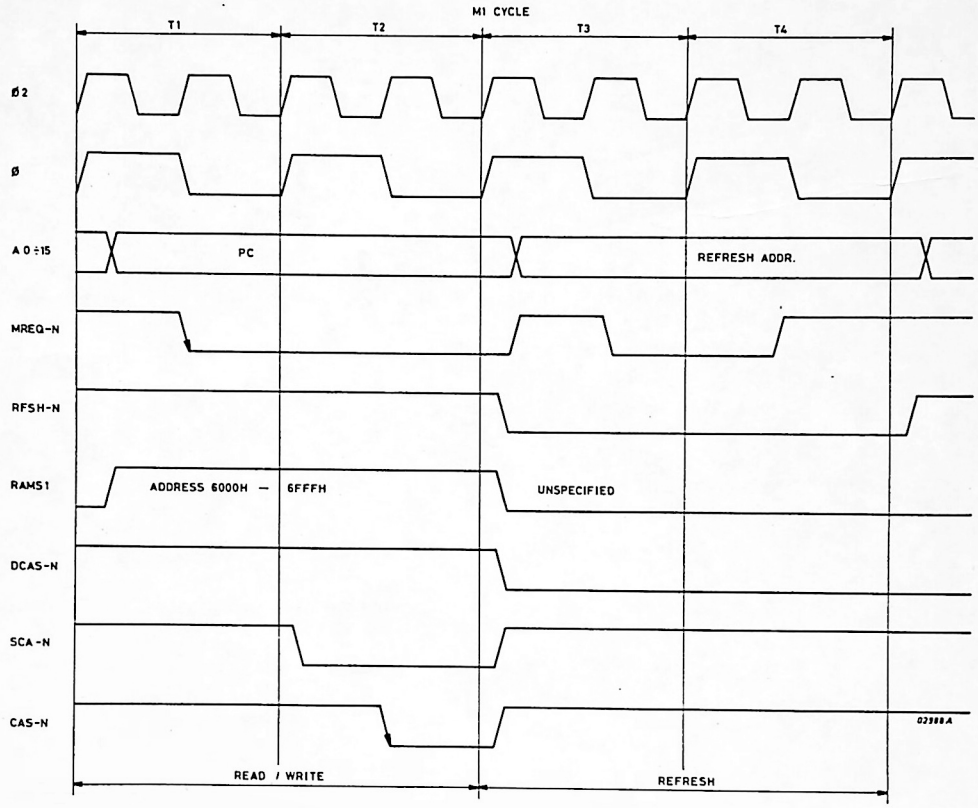

Figure 3.1 RAM TIMING

The MONITOR ROM consists of 2 ROM circuits of 2K8, together forming the monitor program. For further extensions the selection of the ROM's can be changed with help of straps A-D, to implement a 4K8 ROM circuit.
The output of the ROM's, enabled during selection of the monitor ROM, is put to the memory databus (DM0-7). This bus is via a busdriver connected to the CPU-databus. The busdriver is only enabled during memory read actions on ROM or system RAM (MBEN2).

The SYSTEM RAM is formed by 8 circuits of 16K1 each. The multiplexed addressbus (AM0-6) contains either the row address (A0-6) or the column address (A7-13). Data input is directly coming from the CPU (D0-7) while data output is fed via the busdriver to the CPU (DM0-7). The application program is contained in ROM's on a ROM-cartridge inserted via connector to the CPU-board.
Selection of the ROM addresses is done with help of A0-12 and the selection signals CARS1-2, selecting one out of 2 banks of 8K.
The output of the ROM is also fed to the CPU via the DM-bus and the memory busdriver.

3.1.2 I/O CONTROL (FIGURE 4.6.2)

The CPU controls internal and external devices via a number of I/O ports.
On the CPU-board we find the control circuitries for the keyboard, cassette, printer, a bell port for audible alarm and a port to select under software control the priority of video refresh (DISA). The I/O ports are decoded from the address bus according to the next table.

ADDRESS LINES 7 6 5 4 3 2 1 0	SELECTION SIGNAL	PORT NR(HEX)	FUNCTION
0 0 0 0 X X X X	KBS	00-09	Read the key-matrix
0 0 0 1 X X X X	OUTS	10(-1F)	Output to cass/printer
0 0 1 0 X X X X	INS	20(-2F)	Input from cass/printer
0 0 1 1 X X X X	SCRS	30(-3F)	Scroll register (T-version)
-	-	40(-4F)	Reserved for I/O cartridge
0 1 0 1 X X X X	BEES	50(-5F)	Beeper
-	-	60(-6F)	Reserved for I/O cartridge
0 1 1 1 X X X X	DISAS	70(-7F)	DISA port selects priority of CPU or video refresh access to video memory (M-version)

The KEYBOARD CONTROL consists of an 8 bit input port and a BCD-to-decimal decoder.
The keyboard itself is only a matrix of keys, connected between ten x-lines and eight y-lines.
The reading of a key is based on sequential addressing of the ten x-lines and reading of the eight y-lines. Any key suppression results in the interconnection of an x-line and an y-line. (Figure 3.2).

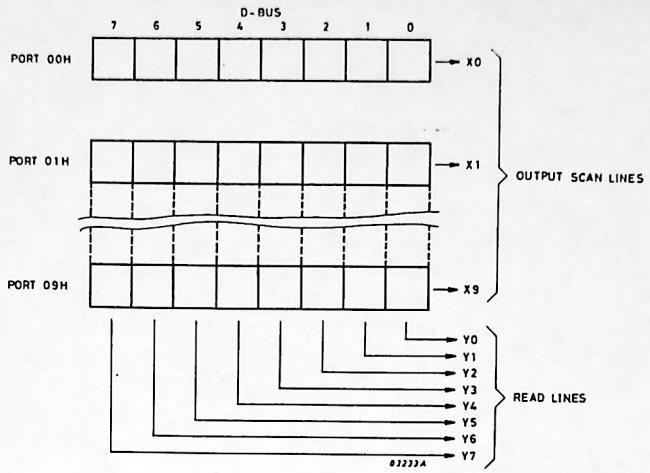

Figure 3.2 KEYBOARD PORT

Scanning of the keyboard is done every 20MS on interrupt-base with help of an INTERRUPT CONTROL circuitry.
This scantime is received from the video timing (signals DEW or R2425-N for T- and M- version respectively).

The keyboard interrupts are only processed if the keyboard interrupts are enabled, which is controlled via a bit of the output control port (KBIEN).

The microprocessor then goes to an interrupt routine and executes a read keyboard action (IN 00). Because of the signal KBIEN being active all x-lines of the keyboard are selected at once via a diode network, forcing all x-lines to logic '0'. (Figure 3.3).

If a keysuppression was made the inputted data will be unequal to FF Hex. The processor then deactivates KBIEN after which the X-lines are scanned sequentially.

At the end of the routine the interrupt is enabled again (KBIEN = '1') to prepare the next 20ms scancyle. The interrupt control on the CPU-board can only handle the keyboard and an external I/O cartridge interrupt.

When the extension board is used also the floppy-controller requires an interrupt process. In this case the interrupt control circuitry on the CPU-board is disabled and the interrupts are generated on the extension board. This is achieved via the signal LOCK-N which is forced logic '0' on the extension board.

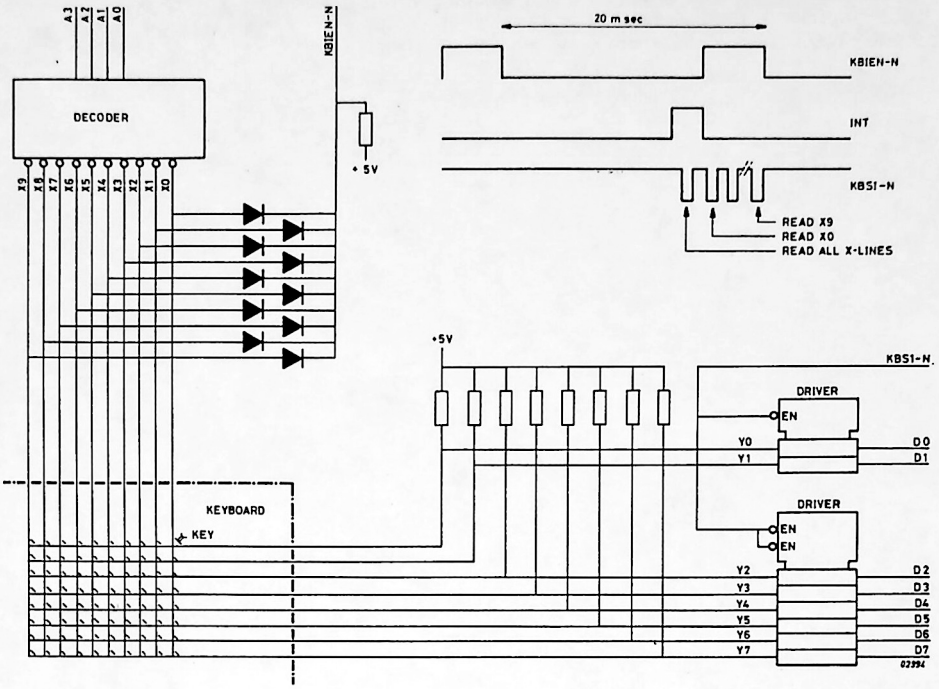

Figure 3.3 KEYBOARD SCANNING

The OUTPUT CONTROL is a port-circuitry to output information to CASSETTE and PRINTER. The selection of port 10H enables the storage of an 8-bit word into 8 output latches. Every outputted bit has a single function according to figure 3.4.

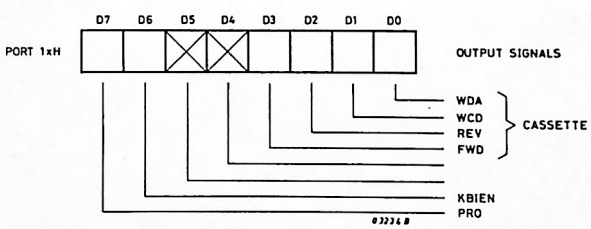

Figure 3.4 OUTPUT PORT (10H)

The CASSETTE is controlled by 4 output lines. Forward (FWD) and rewind (RWD) are two motor control signals to activate the motor in either forward or reverse direction. Data is written to the cassette via the Write Data (WDA) line, which is on the drive enabled when the Write Command (WCD) line is also active. The control of the motor and translation of data to a serial bitpattern in Phase Encoded (PE) format is controlled via routines in the Monitor - Rom.
The printer output control is formed by a single line (PRD), carrying the serial bitpattern of the characters to the printed. The output is passing a TTL/V24 signal convertor to adapt to the V28/RS 232-C signal levels (+12V/+2V). The printer is handled by a monitor-routine which is taking care serializing, addition of start of start/stop bits and parity generation. The speed of transfer is standard 1200bps, but the monitor program is using a speed-control-byte in the system ram which can be varied by the application program to allow the connection of printers operating on other speeds.

The two soldering bridges E and F allow the control of two more interface signals, installed for future adaptions to printers requiring this signals active or not active. The last bit in the output control port is the used for control of KEYBOARD INTERRUPTS (SEE INTERRUPT CONTROL).

The INPUT CONTROL is used to input information from cassette and/or printer. Selection of port 20H inputs 8 bits according to figure 3-5.

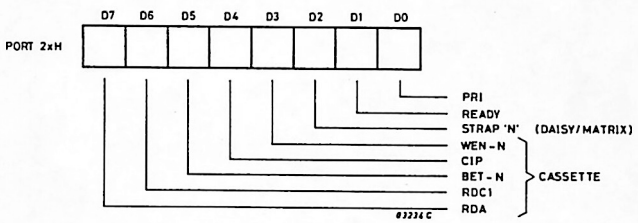

Figure 3.5 INPUT PORT (20H)

The printer control uses two bits.
Printer Input (PRI) is normally not used and only present for testpurpose. Via a V24 convertor this signal is connected to pin 2 of the V24 interface. Ready (READY) is signalling the ready condition of the connected printer. The printer deactivates this signal in case of failures and not operable conditions such as paper out detected.

The ready condition is also checked by the monitor program during data transmission. When the printers is becoming temporaly not ready because of a buffer full condition the transfer of characters is delayed until the printer becomes ready again. (figure 3.6).

Strap N is a hardware strap on the CPU-BOARD via which the selection of either a daisy-wheel printer or a matrix-printer is made. It is used by the monitor program to select the required interface protocol (special character translation etc.)

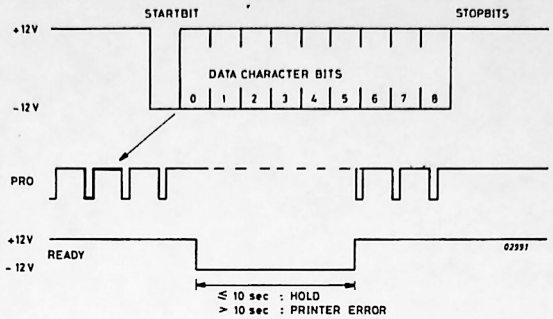

Figure 3.6 PRINTER INTERFACE

The CASSETTE INPUT consists of three status signals, a data signal and a clock signal. The Write Enable (WEN) signal is coming from the switch on the drive which is activated when a write enable plug is added to the cassette medium. Cassette In Position (CIP) is active when a cassette is loaded on the drive and the door is closed. Begin and End of Tape (BET) is signalled by the drive as a condition to stop the tape transport.

The Read Data (RDA) from the cassette is a serial bit pattern in Phase Encoded format. The Read Clock (RDC) is active at start of every new bit. This clock-pulse is triggering the CASSETTE TIMING flip-flop. The flip flop toggles on every clockpulse thus offering a timing signal (RDC 1) in phase with received data. The monitor program checks during a cassette read operation a change of the RDC 1 signal and then loads the value on RDA as a next bit.

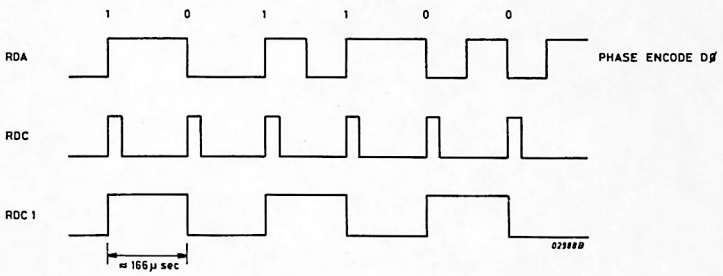

Figure 3.7 CASSETTE TIMING

The PEEPER is controlled via a flip-flop, triggered when port 50H is selected and loaded with the information from bit D0 of the databus. The monitor program gives a number of 0-1-0-1 changes to this port to give an audible alarm. This results for the T- version in an output to the audio channel of the TV and for the M-version the beeper, mounted on the CPU-board, is vibrating.

The DISA port is activated via an output on databit 1 (D1) and the selection of port 70H. It is used only for the M-version to select priority for access to the video memory. When DISA is active the CPU has the highest priority and video-refresh is disabled during CPU access into the video memory.

When DISA is not active the video-refresh has the highest priority (normal situation) and the CPU enters the wait state if access to the memory is wanted. DISA is made active during read operations from cassette and floppy because during this operation an exact CPU timing is necessary and no wait-times for video-refresh are permitted.

PORT 40H and 60H are not wired on the CPU board which allows the allocation of these portnumbers by the I/O cartridge.

3.1.3 VIDEO MEMORY T-VERSION (FIGURE 4.6.3)

The VIDEO MEMORY for the T-version consists of 4 memory chips of 4K1 each, together forming a 2K8 memory area.

The screen image is stored consecutive in the first 1920 location of the memory. The screen memory contains both data-characters and control characters according to the characterset (see P2000 field manual). Bit V0 is the least significant bit and bit V6 the most significant of the 7-bit characters. Bit V7 is used to store the cursor location. The video memory is addressed either by the CPU (CPU-access) or by the video generation logic (VIDEO REFRESH). This is selected by the VIDEO ADDRESS MULTIPLEXOR (VIDS). The signal VIDS is a decoding of the CPU addressbus addressing the video memory (5000H-57FFH). If no CPU-access to the video memory is performed the memory address is offered by a counter circuitry.
In this case the memory address is formed by two parts: a ROW ADDRESS (RA0-4) and a CHARACTER Address (CA0-6).

The 5-bit rowaddress and the 7-bits character address is translated to an 11-bit memory address (AV0-10) by a ROM-decoder, which is part of the address multiplexor. It compose a consecutive memory addressing as follows:

ROW ADDRESS RA0-4	COLUMN ADDRESS CA 0-6	MEMORY ADDRESS AV 0-10
4 3 2 1 0	6 5 4 3 2 1 0	HEXADECIMAL
0 0 0 0 0	0 0 0 0 0 0 0	5000H ┐ ROW 1
0 0 0 0 0	1 0 0 1 1 1 1	504FH ┘
0 0 0 0 1	0 0 0 0 0 0 0	ROW 2
ETCETERA FOR ROW 2-23		
1 0 1 1 1	0 0 0 0 0 0 0	5730H ┐ ROW24
1 0 1 1 1	1 0 0 1 1 1 1	577FH ┘
		5780H - 57FF N FREE

Although the memory can contain 80 characters for every row only 40 characters of each row are displayed.
The SCROLL REGISTER selects which 40 characters out of the memory are displayed on the screen. The scroll register is loaded from the data bus via an OUT instruction to port 30H (SCRS). (Figure 3.8).

The 7 least significant bits (P0-6) are forming the binary number of the first character of every row in memory to be displayed on the screen. Incrementing the contents of the scroll-register has the effect that the total screen is scrolled one position horizontally.

Bit 7 of the scroll-register P7 can be used by the software to disable the display of information on the screen. Information transfer between the video memory and CPU is done via a VIDEO BUS TRANSCEIVER which is enabled during CPU read and write actions into the video memory (VIDS).

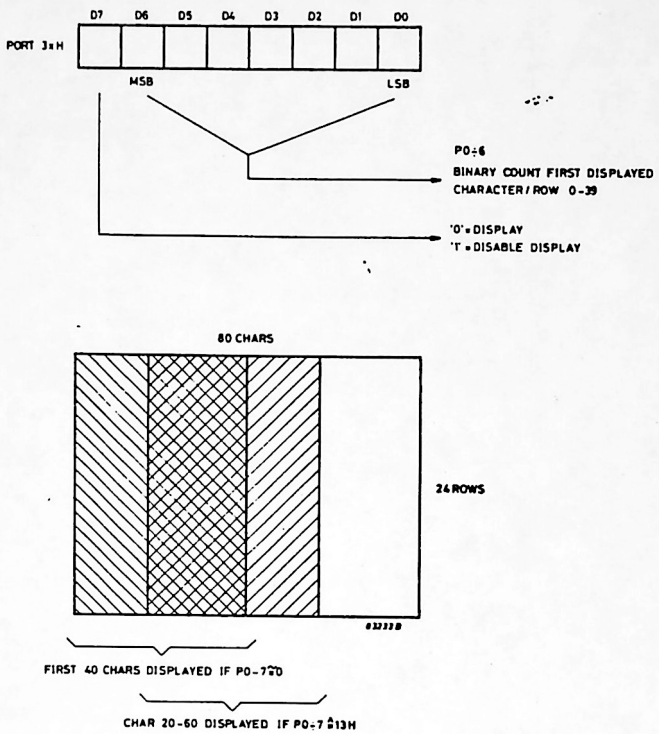

Figure 3.8 SCROLL REGISTER

3.1.4 VIDEO GENERATION T-VERSION (FIGURE 4.6.4)

This section generates the appropriate T.V. timing and video signals to compose a T.V. SCREEN. The TIMING CHAIN consists of a 6MHz scan frequency (F6), the dot frequency. The SAA 5020 circuit generates from this dot-timing the necessary The SAA 5020 circuit generates from this dot-timing the necessary timing for setting up a screen.
The signal F1 is the 1MHz character clock, giving a character time of 6µs to display 6 dots on the screen. The SAA 5020 contains a character counter, counting the number of character times to form one scan line. The total scanline time is 64µs. At character time 6 the line synchronization signal (GLR) is active and during character time the 15-55 the display of 40 characters on the screen is enabled.

During this 40 character times a character clock is offered on RACK, offering every displayable line 40 clockpulses to the character counter. A field rate counter in the SAA 5020 counts the number of scanlines in a field, in our case 313 scanlines. The displayable area of this is from scanline 49 to 289 being 240 scanlines to be used to display 24 rows of 10 scanlines each. The signal CRS is active during the even scanlines of the field. In our system we use only the odd scanlines, so no interlacing is used.

At the end of an odd field signal CRS is activated which is giving via a counter/decoder circuit a new field sync pulse (FS). At this moment again an odd field is started. This gives a total screen-refresh in 20msec (50Hz). The timing chain outputs also a row-address (RA0-4) giving the binary number of the row being displayed (0 - 23). The characters are extracted from the video memory via a VIDEO BUS DRIVER, enabled when no CPU action on the video memory is active (VIDS). Seven bits of the character are entering the CHARACTER GENERATOR (CR0-6). This circuit generates from the character code a serial dot pattern. The video outputs are signals y (monochrome video) B (blue), G (green) and R (Red).

Several versions of this character generator are available, for the display of various national version characters. (SAA5050, 5051, 5052).

The character set includes alphanumeric codes in a 5x7 matrix and graphic codes in 6x10 matrix (Figure 3.9). The character generator decodes also the specific control characters, selecting special features as CHARACTER/GRAPHIC selection, display colour/background colour, double bought characters flashing characters etc.

Selection of double height characters in the character generator is signalled back via TLC to the timing chain which is then counting 20 scanlines per row. The screen is blanked via input DE inactive, which signal is coming from bit P7 of the scroll-register. Display of the cursor is controlled via a separate circuitry INVERSE VIDEO control.

The cursor information is stored in bit 7 of the video memory (CR7). When this signal is active it inverts the outputs of the character generator via an exclusive or gate.

The information which is now formed can be sent directly to a special Television Set adapted with a RGB-interface. This interface requires only a composite sync-signal, (SYNCH) the three colour signals (R,G,B) and the signal BEEP for audible alarm.

For connection at a standard TV the information is first modulated on a MODULATOR PCB. This modulator outputs a VHF - or UHF - modulated video signal. The modulator requires, apart from video signals also a burst - signal and PAL frequency for the compatibility to either PAL or NTSC modulation systems.

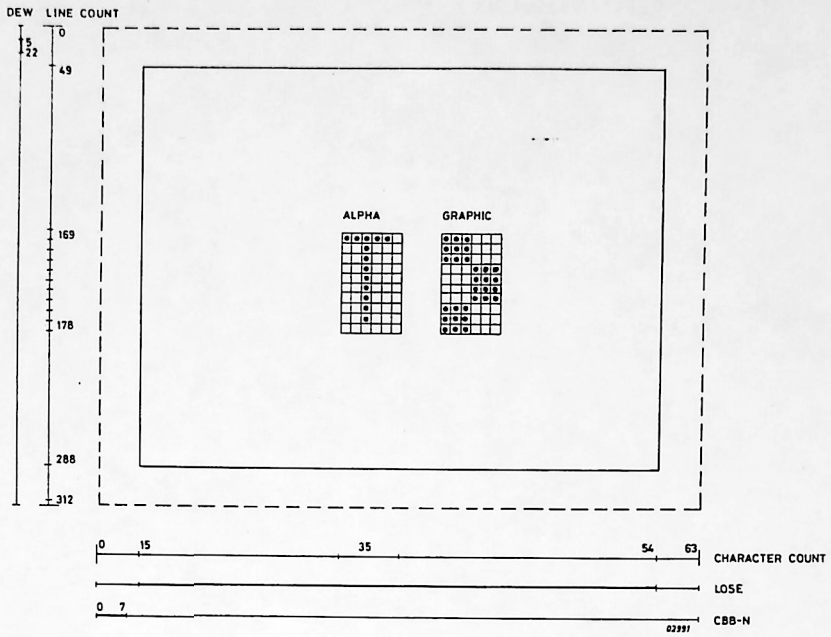

Figure 3.9 VIDEO TIMING (T)

3.2 VIDEO BOARD (M-VERSION FIGURE 4.7)

This board is used only in the M-version to control the professional video monitor of the monitor cabinet. In this case the CPU-board does'nt provide the video memory and video generation logic.

The video board can be splitted in four functional parts:

- BUS control
- Video Timing
- Video Memory
- Video Generation

3.2.1 BUS CONTROL FIGURE (4.9.1)

The video memory is selected in two ways:
The CPU addresses either the video memory of 2K8 containing the characters or the 2K4 memory containing the attributes (VIDSEL). The screen is refreshed by addressing the video memory for both character and attributes as a 2K12 memory (REFSEL) (Figure 3.10).

The VIDEO MEMORY DECODER decodes the address for selection of both video and attribute memory with signal VIDS (5000 H-5FFFH).
The BUS CONTROL selects a data transceiver into read mode (DBRDU) on the conditions of reading from video or extension RAM (RAMRQU), read from I/O ports on the extension board (IORQU, port 80H-FFH) of a read from the interrupting device on the extension board (INTA).

The bus control logic enables also the bus transceivers of either video or attribute memory during data transfers between CPU and memory. (DBENA, DBENV).
The REFRESH CONTROL circuitry is used to generate an access to both video and attribute memory when new information is needed by the video generation. The refresh action is done once for displayed row, controlled by timing signals from the video timing (L11, C0490). During scanline 11, character time 4 up to 90 of every row the signal REFSEL is active, indicating a screen refresh action. A special circuitry is provided in this logic to prevent that both screen refresh access and CPU access is made to the video memory. This is controlled via signal DISA from port 70H of the CPU board.

When the signal DISA is active the CPU access to the video memory has the highest priority and the information which is going to be displayed is temporaly wrong. When the signal DISA is made inactive the screen-refresh has the highest priority. If now during screen refresh (LIN11) the CPU attempts for a data transfer a WAIT signal is activated which forces the CPU into wait mode as long as LINE 11 is active.

The CHIP SELECTION VIDEO MEMORY selects out of 4 banks of 1K video memory. CS 1, 2 select the video data memory (5000-57FFH) and CS 3,4 select the video attribute memory (5800H-5FFFH). The chip selects signals are decoded from the video address bus (VA10-11). During CPU access the banks are addressed separately but during video refresh both attribute and data has to be accessed at once. This is done with help of the multiplex circuitry selecting either CS3 (normally) or CS1 (during screen refresh) to be the selection signal for the attribute bank (CS31)

So during refresh actions (LIN11) the signals CS1 and CS31, or signals CS2 and CS 42 are active.

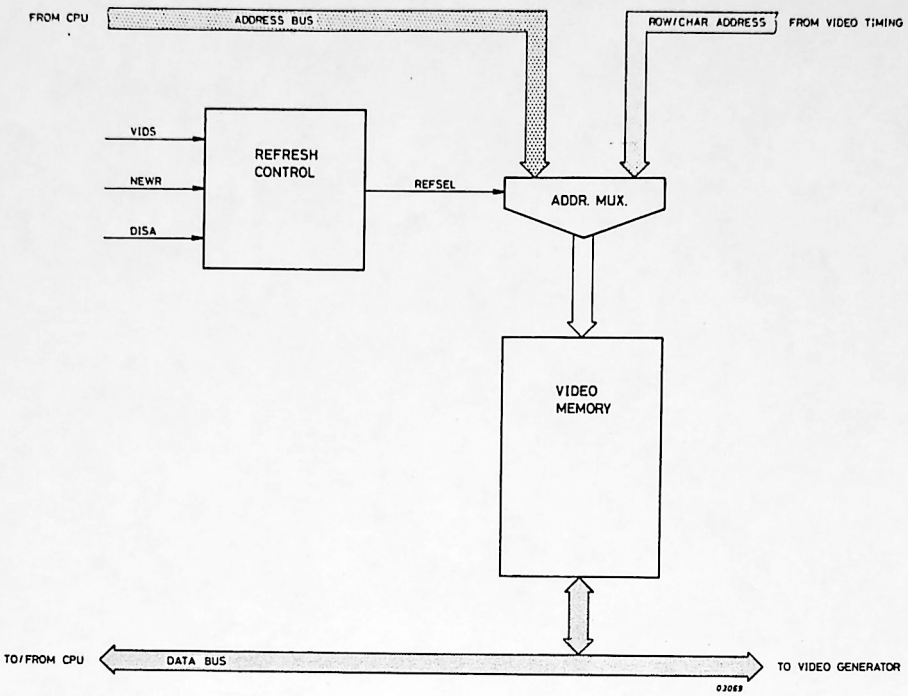

Figure 3.10 VIDEO MEMORY ACCESS

3.2.2 VIDEO TIMING (FIGURE 4.9.2)

The VIDEO TIMING offers the necessary timing signals to generate a screen. (Figure 3.11). The timing is derived from a crystal clock generating a 12MHZ dot-timing (V12M).

The dot timing triggers a DOT COUNTER which is counting 8 dots to display a complete character, including the spacing between the characters (DC0-2).
The dotcounter position 7 and 0 are decoded in the DOT DECODER to be used for internal timing purposes.

Every 8 dots (DOT 7) the CHARACTER COUNTER is triggered, counting with two counter circuits, 96 character times to display a complete scanline of the screen (CC0-6).
The CHARACTER DECODER outputs a number of timing signals to be used by the video generation logic. C0686 is the displayable area on the screen, during this 80 character times video display is enabled. From character time 4 up to 90 (C0490) the video memory is addressed for screen refresh to fetch a new row of information. Characters are loaded from memory into video generation logic during character counter positions 0 upto 85 (C085). The HOSY signal synchronizes the monitor electronics horizontal deflection signal from character 92 to 0 or 16, which is strap selectable to allow the connection of several monitor types.

Every last character time of a scanline (C95) the LINE COUNTER is triggered, which counts totally 12 scan lines to display one row of information (LC0-3). The LINE DECODER decodes the last line of a row (L11) which is used to reset the line counter and during this scanline also new information is fetched from memory for screen refresh. LINE 9 is used in the video generation to enable the display of an underline.

Every last scanline (L11) the ROW COUNTER is triggered, counting with a 5 bit counter totally 26 row times to compose a screen (RC0-4). At the end of row 25 the counter is synchronously reset with signal R2425. This signal appears every 20ms, the total screen time, and is used also as timing signal for the interrupt logic (KEYBOARD).

The ROW DECODER outputs the signal VESY for vertical synchronization of the monitor electronics which is derived from row 24 (R24). Vesy is active at the trailing edge of R24, so at the end of row 24 (last displayed row) a vertical flash back is started. A soldering bridge is available to allow for the connection of a monitor with active-high going vesy pulse. The signal NEWR takes care for loading new row information during the 24 displayable rows.

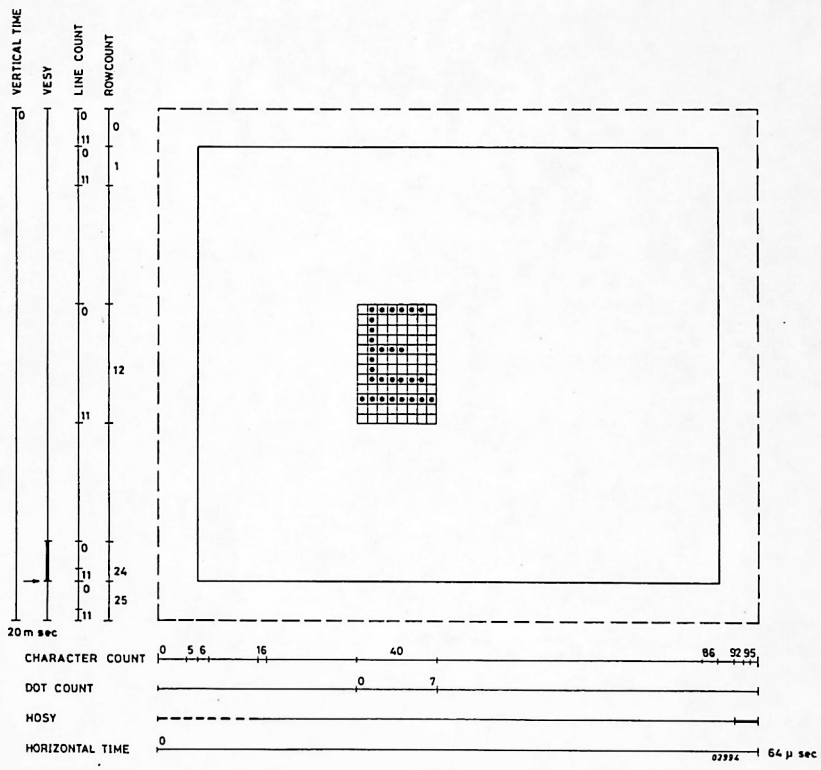

Figure 3.11 VIDEO TIMING (M)

3.2.3 VIDEO MEMORY (FIGURE 4.9.3)

The VIDEO MEMORY consists of 2 parts. The PAGE MEMORY ATTRIBUTES consists out of 2 circuits of 1K4 forming a 2K4 memory area. The 4 bits contain graphic (DGRA), underline (DU) blinking (DBLI) and inverse (DINV) information. (Figure 3.12). The memory is loaded via the video bus transceiver from data bit DU0-3 respectively, enabled during CPU access with signal DBENA.

The PAGE MEMORY VIDEO consists 4 circuits forming a memory array of 2K8. The seven least significant bits contain the character codes to be displayed (DU0-6), while the last bit contains the cursor information (DCUR). CPU load and store actions into the memory are transferred via the video BUS TRANCEIVER from the CPU databus (D40-7) which is enabled with signal DBENV.

The VIDEO ADDRESS MULTIPLEXER selects either the CPU address or a refresh address to be offered to the memory, controlled via signal REFSEL.
The refresh address is offered by the ADDRESS COUNTER (AC0-11), formed by these 4 bit counters.
The counter control resets the counter (ACRES) at the begin of row 24 (LASTR). This results in fetching the information for ROW 1 at line 11 of row 24.

During refresh, happening every Row in line 11, the counter is stepped 80 times (C0585) thus offering a consecutive memory address to both the video and attribute memory (ACCL).
The ADDRESS and DATABUS DRIVER are used to increase the fan-out of the CPU busses.

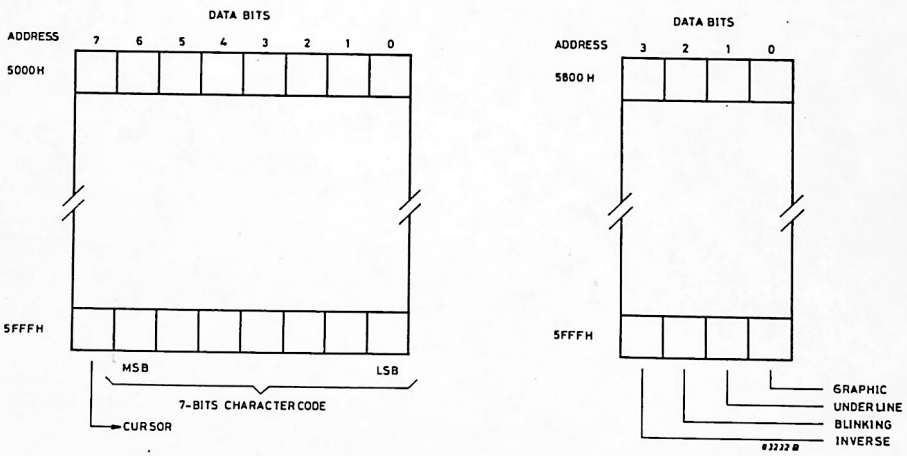

Figure 3.12 VIDEO MEMORY LAYOUT

3.2.4 VIDEO GENERATION (FIGURE 4.9.4)

The ROW MEMORY VIDEO and ROW MEMORY ATTRIBUTES are loaded every last scanline of a row with the information of the next row from memory. The ROW MEMORIES consists of 12 dynamic shift register memories of 80 bits each. The memories are clocked each scanline during character time 5 up to 85 bits (RMCL). Normally the memory is circulating, so the character which is outputted is also shifted back to the input. Only during scanline 11 new information is shifted in while the old information is shifted out. (NEWR).

The output of the video row memory is latched in the character latch (RMB0-6) and offered to the character generator. The last bit of the video row memory is not going to the character generator but is now forming an attribute for the video mixer (RCUR). One bit from the attribute row memory contains graphic or character selecting information (RGRA). This bit is offered via the CHARACTER LATCH to the character generator.

The character generator consists of 2 circuits, one for the upper 8 scan lines of a row and one for the lower 4 scanlines. It converts the coded information from the row memory to an 8 bit dot pattern for every scan line of the character to be displayed. This is achieved with two ROM circuits containing on every location a dot code. The ROM is addressed by the character code (RM80-6) the graphic or alpha bit (GRA) and the line counter (LC0-3).
The character generator can also be found by one ROM circuit of 4K8.

The dot pattern (VID0-7) is every character time (DOTO) loaded into the VIDEO SHIFT REGISTER and shifted out as a serial video data (VIDATA) every dottime (V12M). The three other attributes, together with the cursor bit, are passing two ATTRIBUTE LATCHES to offer this signals at the same timing moment to the video mixer.

The VIDEO MIXER mixes the attributes to the serial video. When attribute underline or cursor is active during line 9 the video information is made active (ULCU9, DAUC). When either the cursor (CUR9) or the blinking (BLI) attribute is active (BLICUR) the video information is blanked in a blinking frequency (BLIFR) offered by a timer circuit. The video information (VIDINF) is inverted when the inverse attribute is active (INV) via an exclusive or gate. This information is then anded with the displayable area of the screen (C0686 R0124) and offered to the monitor electronics (VIDEO).

3.3 EXTENSION BOARD (FIGURE 4.10)

The extension board offers two options to the P2000:

- memory extenstion
- floppy controller

3.3.1 MEMORY EXTENSION (FIGURE 4.12.1)

The memory extension provides 1 or 2 memory banks, BANK0 and BANK1, to extend the RAM memory with maximum 2 X 16K8 RAM. A memory bank consists of 8 dynamic memory cells of 16K1 each.

The memory uses multiplex addressing, the address being offered in two steps, firstly a 7 bit row address and then a 7 bit column address, controlled via the ADDRESS MULTIPLEXER. (SCA) The memory in and output pins (DM0-7) are wired via the MEMORY BUS TRANSCEIVER to the tri-state databus on the extension board (DE0-7).

The databus on the extension board is connected via a DATA BUS TRANSCEIVER to the CPU-databus (D0-7) in the T-version, or to the video-board (DU0-7) in the M-version. The address bus is coming from the CPU-board (A0-14, RAMS2) in the T-version, or via the video board (AU0-14, RAMSU) in the M-version.

The BUS DRIVER provides a high drive capability for part of the address bus (AE0-7) and CPU-control signals (WRE etc). The ADDRESS DECODER decodes the most significant line of the address bus to select bank 0, from A000N up to DFFF H (BS0) and bank 1 from DFFFH up to FFFFH (BS1). This last area of RAM (BS1) allows only a direct CPU addressing of 8K memory.

To access also the upper 8K in this bank a programmable signal (RAMSW) is avialable which is offering for bank 1 the signal SEL8K as the upper address line to memory. During selection of bank 0 the signal SEL8K carries the address bit 13 (A13). Signal BS10 is active during selection of either bank 0 or 1. The signal IOE provides the selection of 1/0 ports on the extension board. It is directly related to address line 7 (port 80H to FFH).

The MEMORY TIMING circuitry delivers the required signal for multiplexed addressing of the RAM BANKS during CPU-access, and A RAS-only cycle during memory refresh (Refer to 3.1.1).

The BUS CONTROL enables the memory bus transceiver during access from the extension memory (MRDE) and selects the DATA BUS TRANSCEIVER for read mode during memory read, I/O read or interrupt vector read operations (RDE).

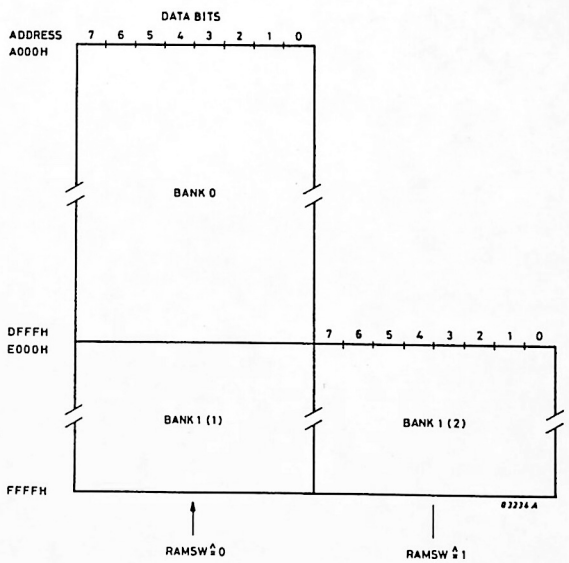

Figure 3.13 EXTENSION MEMORY LAYOUT

The DEVICE SELECTION logic delivers the required decoding for selection of the I/O ports on the extension board according to the next table:

PORT NUMBER	SELECT SIGNAL	DEVICE
88H - 8BH	CTCSEL	COUNTER/TIMER Z80-CTC
8DH - 8FH	FDCSEL	FLOPPY CONTROLLER µPD765
90H	IOPSEL	FLOPPY/DC CONTROL PORT
94H	SWSEL	RAMSWITCH MEMORY BANK 1

Output port 94H selects a Flip-Flop (RAMSW) which is set when databit D0 is active. The address now offered by the CPU selects the upper 8K of the RAM BANK1. Output of a byte with bit D0 low reset the flip-flop after which the lower 8K of the BANK is selected. During output to port 90H the signal OUTSEL is active and during input port 90H the signal INPSEL is active.

3.3.2 FLOPPY CONTROL (FIGURE 4.12.2)

The main circuit to control the floppy disk drive is the intelligent FLOPPY CONTROLLER (µPD765). This controller can execute autonomously a number of commands such as search, format, Read track, Write Track etc. The controller performs this actions in three phases:

- COMMAND PHASE
- EXECUTE PHASE
- RESULT PHASE

In the command phase the controller is loaded with the command code and a number of variables. To do this first the main status register of the controller is read by reading from the controller (FDCS, FCRD) and signal FSTA active (A0 = 0). After that the bytes are written to the controller (FCS, FCWR).
During execute phase the controller activates for every data transfer to /from the CPU the signal DRQ (DMA-mode). The floppy controller is designed to operate in semi-DMA mode.

The signal DRQ is scanned by the floppy controller software during the execution phase of a Read or Write command, via a read of port 90H (INPSEL)
The signal DMA-request (DRQ) has to be answered with a DMA-acknowledge (DACK). This is realized by a read or write action to the controller with signal FCDK active. In this case no chip selection signal (FCS) is required.

When the execution phase is terminated, either by the controller itself or on request of the CPU (signal FCTC, terminal count) active, the controller is going to the result phase. On this moment an interrupt is raised (INT) which is processed by the interrupt controller and results in the execution of a floppy interrupt routine.

In the result phase one or more status bytes are read from the floppy controller by the CPU (FCS, FSTA, FCRD active).
The output port is selected when an OUT 90H instruction is executed. The four least significant bits of the output data are then stored in an output latch.
Bit 0 is used for selection of either data transfer or command/status transfers to the controller. (BIT 0 = 0 means command/status, BIT 0 = 1 means data transfer)
Bit 1 is used for prematurely termination of commands. (BIT 1 = 1 means Terminal count)
Bit 2 is used to select either reset or enabling of the floppy controller.
(BIT 2 = 1 means enable, BIT 2 = 0 means reset)
Via Bit 3 of the output port the motor-on signal to the floppy drive is controlled.
(BIT 3 = 1 means motor-on)
The INPUT PORT is selected when a IN 90H instruction is executed.
Only BIT 0 is used of this port to input signal DRQ (data-request).

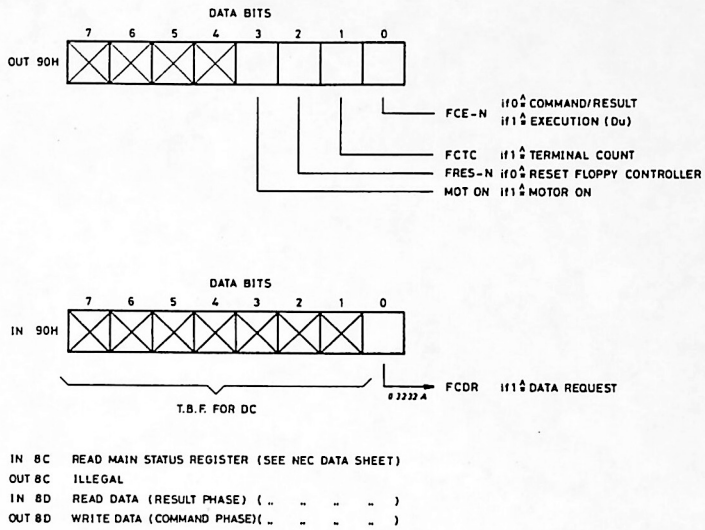

Figure 3.14 FLOPPY CONTROL PORTS

The FLOPPY TIMING circuitry offers the WRITE Clock for the controller (WCK) and a timing signal used in the read logic (T42).
The controller is designed for MFM operation (MODIFIED FREQUENCE MODULATION) signal MFM. This selects a read recovery timing signal of 4MHz (T4M and a write Clock of 500KHZ (WCK)

The WRITE CONTROL logic is used for precompensation of the write data signal (WRDATA) giving phase shifts of the write data in steps of 250 ns. Selection of early (WDAE), normal (WDAN) or late (WDAL) is coming from the floppy controller (PS0,1) and depends of the pattern of data to be written on the diskette.

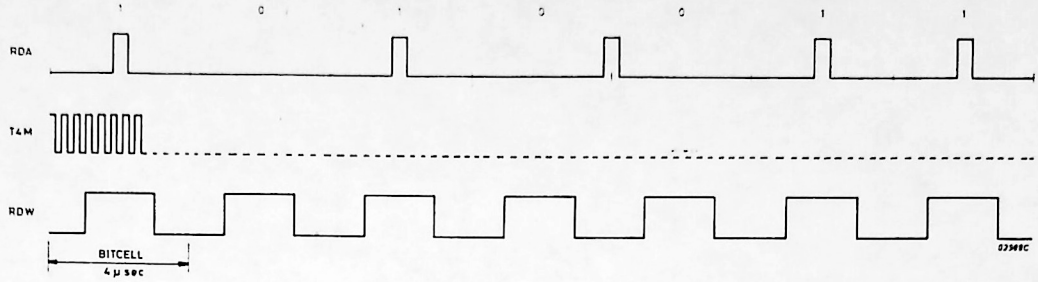

Figure 3.15 DATA RECOVERY

The STEP CONTROL circuitry is a multiplexing circuitry offering in R/W mode the write protection signal from the floppy-drive (WP/TS) while in seek mode the TRACK-00 detection is inputted (FLT/T90) and the step control signals direction (DIR) and step commands (STEP) are offered to the floppy drive. The DRIVE SELECT circuitry decodes the unit select signals from the controller (US0,1) to select either drive 1 or drive 2 (DRISEL 1,2).

The READY CONTROL circuitry generates a not ready interrupt (FNR) if no index pulses are detected after activation of the floppy-drive (HDL). Thus it detects if the diskette is entered, the door closed and the motor is running.

The INTERRUPT CONTROLLER consists of a programmable COUNTER/TIMER circuit (Z80-CTC). The circuit is programmed via selection of port 8CH to 8FH. It provides four channels, selected with address line 0 and 1 (AE0, 1).

Channel 0 has the highest priority and is programmed to give an interrupt when the clock/trigger input becomes active (FCINT). The interrupt is offered to the CPU (INT-N) which is operating in interrupt mode 2. This results in an interrupt cycle of the CPU, indicated with signal M1 and IORQ active together. The controller offers now a byte to the CPU which contains the, previously programmed, interrupt vector of the interrupting channel. With this information the CPU can branch to the required interrupt service routine, in this case the floppy controller interrupt routine.
A similar action is happening when the floppy becomes not ready, controlled via channel 1 (FNR).

Channel 3 is again programmed in interrupt mode to offer the necessary keyboard scan interrupt every 20ms.

The READ TIMING circuitry (Figure 4.12.3) synchronizes a read data window (RDW) to the read data from the drive (RDA).
The middle of this window indicates to the floppy-controller the begin and centre of a bitcell (Figure 3.15).
The read timing circuitry is released just before the data is expected from the drive.
This appears when the signal VCC from the drive is becoming active. The information from the drive (RDA), containing both clock and data information is first shaped in a one-circuitry (RDA1).

The timing of the datawindow is now compared with the incoming information, by latching the phase-difference in two flip-flops (DEARLY AND DLATE).
The amplifier circuitry µA741 generates from these pulses a DC-voltage (PHASE DIFF.), the level of which depends on the phase difference between data and window.
This DC-level corrects the frequency of the datawindow untill the phase difference is minimal. This is realized with a voltage controlled oscillator (4024), generating the datawindow via a divider circuitry.

3.4 POWER SUPPLY

This section describes the power supply boards of the basic and monitor cabinet.

3.4.1 POWER SUPPLY BASIC CABINET (FIGURES 4.13/4.14)

The transformer supplies a voltage which is rectified via D1 and D2 and smoothed at capacitor C1 and C2. The voltage is then via three separate regulator circuits offered to the three boards of the basic cabinet. Regulator 1 and 2 are interconnected for the T-version to increase the +5V output power. The voltages of winding S2 are rectified via rectifier bridge D3.

By using the middle tab of the winding this results in the generation of a positive voltage over C3 and a negative voltage over C4.
The positive voltage is via regulator circuit 4 directly offered as +12V to all boards. The unregulated - voltage (-20V) is directly supplied to all logic boards. An every board this voltage is regulated to supply - 5V and -12V.
Transistor TS1 and TS2 are forming a protection circuitry for the +12V supply. As long as the +5V is not available TS1 is non-conducting and TS2 is conducting. Thus the +12V is short-circuited as long as the +5V fails.

3.4.2 POWER SUPPLY MONITOR CABINET (FIGURES 4.15/4.16)

The +5V supply for the FLOPPY DRIVES is derived from rectifier D1 via regulator circuit IC1. This voltage is also driving the power-on led of the cabinet. The voltage of the second winding from the transformer is rectified by a diode-bridge formed by D2 - D5 and smoothed with capacitor C14, 15, 16. IC3 regulates a voltage of +12V to be supplied to the monitor electronics. The +12V supply for the floppy - drive is regulated with IC1 and power-transistor TS1. The voltage is sensed via R2, R3, R4 and fed back to the regulator. The +12V supply is adjustable with R4.

3.5 ROM CARTRIDGE BOARD (FIGURES 4.17/4.18)

This plug-in module consists of a PCB to which up to 4 ROM-circuits of either 1K8, 2K8 or 4K8 program memory can be inserted. The address is offered via a bus driver. A binary to decimal decoder is used for chip-selection of the ROM-circuits. Soldering bridges A to I are used when ROM-type 2532 is used, to obtain pin-compatibility. Normally bridges 1 to 9 are soldered.

3.6 I/O CARTRIDGE BAORDS

3.6.1 VIEW DATA INTERFACE BOARD (FIGURES 4.19/4.20)

This board offers and interface to an asynchronous modem operating at 1200 B/S. The facility to send data from the P2000 via a backward channel at 75 B/S offers the possibility for a switched connection to the VIEW DATA systems. The main logic circuit on the PCB is the 8251 USART (IC11).
This programmable circuit interfaces between the systems databus and the serial V24 modem interface.

The USART is selected by the P2000 - CPU via decoder circuit (IC10) which is decoding addresslines A4 - A7 during an I/O instruction. The USART contains several registers, which are selected with this decoder and the command/data input, (wired to addressline A0).
This results in the next table for access and operation of the USART:

OUT 41	(after RESET) LOAD D0 -	D7 INTO MODE REGISTER (used to select char. format, parity etc)
OUT 41	(other times) LOAD D0 -	D7 INTO COMMAND REGISTER (used to activate transmit/receive actions)
IN 41		READ USART STATUS REGISTER (used to check on correct receive/transmit)
OUT 40		LOAD DATA INTO TRANSMIT REGISTER (character to be transmitted)
IN 40		READ DATA FROM RECEIVE REGISTER (fetch received character)

Circuits IC2 and IC3 are used to convert the modem interface levels (+12V/-12V) to TTL-level. The USART requires a transmission clock of 16x the actual bit-rate which is achieved by dividing the system clock Ø (2.5 MHZ) by 130 with help of IC 4,5 resulting in clock frequence of 16X 1200 BD. The circuit IC6 gives another 16 x division, thus offering the required clock of 16x75 HZ for the backward channel transfers. Selection of either normal transfer (2x1200 B/S) or backward channel transmission (viewdata) is software controlled via IC 8.

This two-bit register is loaded from the databus with an OUT 60H instruction, the address bus again being decoded via IC10. Bit 6 active selects multiplexer IC9 to offer the reduced transmit clock to the USART while modem signal CT106(CTS) is ignored, and forced active. Bit 7 is used to activate the backward channel modulator (RTS2, PIN19) before the characters are sent.

3.6.2 SERIAL INTERFACE BOARD (FIGURES 4.21/4.22)

The serial interface board can be used as a general purpose communication interface. This board offers some other features then the viewdata interface board described above. The USART 8251 (IC2) is a progammable controller for both asynchronous and synchronous control. It controls, apart from serializing an desserializing of data, most of the V24 modem control signals such as DTR, DSR, RTS and CTS.
Via a separate input port (IC3) the software can check the presence of some other control signals (DCD (8) and CIN (22).

The USART can be clocked either internally (strap 8,9) or externally (strap 7,10), however the external timing signals are not wired to the modem connector (TxC, pin 15 and RxC, pin 17).

The internal timing is derived from the systems clock Ø via a divider circuitry (IC 8,9). Switches S1 are used to select the required speed, closing one of the switches selects one timing out of a range of possible speeds.
The port selection on the board is performed by a binary to decimal decoder of address lines A4 - A7 (IC7). A decoding of binary 4 on these addresslines selects the USART.

On the USART addressline A0 is wired to the C/D input which results in the same table as for the viewdata board:

OUT 40	WRITE DATA TO LINE
IN 40	READ DATA FROM USART
OUT 41	SET USART MODE (AFTER RESET)
	SET USART COMMAND (NEXT TIME)
IN 41	READ USART STATUS

The decoder output 6 enables the other ports on the board, together with a decoding ot A0 and A1 this results in:

IN 61	READ STATUS PORT (DCD, CIN)
IN 62	READ GENERAL PURPOSE STRAPS

The last port is used to read a strap bank S2 via which the system can be informed about things like transmission type, required parity etc.
This strapping depends of the application and are accessable by the user.

3.7 SIGNAL NAMES

A0 -15	16 bit address bus
AC0-11	Screen Refresh Counter (0-1919)
ACCL	Address Counter Clock
ACRES	Address Counter Reset
AE0-7	Address Bus from CPU board (T-version) or Monitor board (M-version)
AM0-6	Memory Address Bus
AM0-7	Multiplexed Address Bus
AU0-14	Address Bus to Upper boards
AV0-10	Address Bus to Video Memory
BEES	Beeper Select
BEEP	Activate the audible alarm
BET	Begin or End of tape
BS0	Bank Select 0 (A000H-DFFH)
BS1	Bank Select 1 (E000H-FFFH)
BS10	Bank Select 0 and 1
C95	Character 95 (last character)
CA0-6	Character Address
CARS 1	Cartridge selection 1 (1000H-2FFFH)
CARS 2	Cartridge selection 2 (3000H-4FFFH)
CAS	Column Address Strobe
CAS 0	Column Address selection bank 0
CAS	Column Address selection bank 1
CC0-6	Binary Court - Character Counter (- 96)
CIP	Cassette in position
C0585	Character 5 up to 85
C0686	Character 6 up to 86
CR0-6	Video Memory Data
CS 1, 2	Chip Select 1 and 2 - Video Memory
CS24, 13	Chip Select 3 and 4 - Video Attribute Memory
CTC SEL	Select Z80 CTC (Port 88-8B) timer
D0-7	8 bit bi-directional data bus
DBENA	Data Bus Enable Attribute Memory
DBENV	Data Bus Enable Video Memory
DBRDU	Data Bus Read Enable Attribute Memory
DBLI	Blinking Attribute
DCUR	Cursor Attribute
DC0-2	Binary Count - DOT Counter
DE0-7	Data Bus on Extension Board
DBENA	Data Bus Enable Attribute Memory
DBENV	Data Bus Enable Video Memory
DBRDU	Data Bus Read Enable Attribute Memory
DBLI	Blinking Attribute
DCUR	Cursor Attribute
DC0-2	Binary Count - DOT counter
DE0-7	Data Bus on Extension Baord
DEW	Data Entry window. Active during scan line 5 to 22 (20msec)
DGRA	Graphic Attribute
DINV	Inverse Attribute
DIRECTION	Define Head Direction
DISA	Disable Access
DISPS	Disable Refresh Selection (M-version)
DM0-7	Memory Data Bus, bi-directional

DOT 0	Dot 0 (first dot)
DOT 7	Dot 7 (last dot)
DUL	Underline Attribute
DUO-7	Data Bus to upper boards
DVO-6	Data Character to Row Memory
FCDK	Floppy Controller Data Acknowledge
FCDR	Floppy Controller Data Request
FCINT	Floppy Controller Interrupt
FCRD	Floppy Controller Read Control
FCTC	Floppy Controller Terminal Count
FCWR	Floppy Controller Write Control
FDCS	Floppy Disk Controller Chip Select
FDCSEL	Select UPD 765 FDC (Port 8C-8F) floppy controller
FNR	Floppy Not Ready
FRES	Floppy Controller Reset
ESTA	Floppy Status - Register Selection
FWD	Forward
GLR	General Line Reset
HOSY	Horizontal Synchronization
INDEX	Index pulse detection
INPSEL	Select Input Port (Port 90)
INS	Input Selection (I/O decoder)
INSEL	Input Selection (floppy disk controller)
INT	Interupt Request
IOE	Input/Output enable extension bard (Port 80-FFH)
IORQ	Input/Output Request
INVERT	Inverse Video Control
KBS	Keyboard Selection
KBIEN	Keyboard Interrupt Enable
LIN 11	Line 11 (last line)
LOCK	Disables Interrupt generation if extension board is used
LO-3	Binary Count - Line Counter
LOSE	Load Output Shift Register
MBEN	Memory Bus Enable
MBEN 2	
MOTON	Motor On
MRDE	Memory Bus Read Enable
MREQ	Memory Request
NEWR	New Row
NMI	Non Maskable Interrupt
Ø	2,5 MHz Clock
Ø2	5 MHz Clock
OUTSEL	Select Output Port (port 90)

PRO	Printer Output
PO-6	Preset value of the character output
P7	Enables display of Data and Cursor
RO124	Row 1 to 24 (displayable rows)
R2425	Row 24 and 25
RAO-4	RAM Row Address
RACK	Read Address Clock
RAMS1	Random Access Memory Selection 1 (6000H-9FFFH)
RAMS2	Random Access Memory 2, Selects RAM on Extension board (A000H-FFFFH)
RAMSU	RAM select Upper Board
RAMSW	RAM Switch
RCO-4	Binary Counter (÷ 26)
RD	Read
RDA	Read Data
RDA-2	Read Data, synchronized with T4M
RDC	Read Clock
RDE	Data Bus Read Enable
RDW	Read Data Window
RDWR	Read or Write
READY	Printer Read
REFSEL	Screen Refresh Selection
RES	Reset Signal
RESA	Reset Switch
REV	Reverse
RFSH	Refresh
RMCL	Row Memory Clock
RMDO	Data Character from Row Memory
RMD7	Cursor Information from Row Memory
ROMS1	Read Only Memory Selection 1 (0000H-07FFH)
ROMS2	Read Only Memory Selection 2 (0800H-0FFFH)
SCA	Select Column Address
SCRS	Scroll Register Selection (T-version)
SEEK	Head movement operation
SEL8K	Selects upper 8K of bank 1
STEP	Causes head to move one track
TRK00	Track 0 detection
T4M	4MHz clock
US0,1	Unit Selection 0 and 1
VO-7	Video Data Bus
V12M	12MHz Video Timing (Dot Clock)
VESY	Vertical Synchronization
VIDO-7	Video dots 0-7
VIDATA	Video Data
VIDEN	Video Page Memory Enable
VIDEO	Video Signal
VIDS	Video RAM Selection (T-version)
VIDSEL	Video Memory Selection
VIDWR	Video Memory Write Enable

WAIT	Wait Request
WCD	Write Command
WDA	Write Data
WE1,2,3,4	Write Enable memory chips (5000H-55FFFH)
WEN	Write Enable
WPROT	Write Protocol - Disk detection

X0-X9	Output to the ten scan lines of te keyboard matrix

Y0-Y7	Input from the keyboard matrix
Y1	Video Output Monochrome
Y2	Video Output Blue
Y3	Video Output Green
Y4	Video Output Red

3.8 INTERCONNECTIONS (FIGURE 4.3)

3.8.1 CPU - BOARD TO VIDEO OR EXTENSION BOARD

1	L	21	A10
2	D	22	A11
3	D0	23	A12
4	D1	24	A13
5	D2	25	A14
6	D3	26	RAMS2
7	D4	27	MRQ-N
8	D5	28	RD-N
9	D6	29	INT-N
10	D7	30	WR-N
11	A0	31	IORQ-N
12	A1	32	WAIT-N
13	A2	33	M1-N
14	A3	34	RES-N
15	A4	35	LOCK-N
16	A5	36	RFSH-N
17	A6	37	DEW/R2425 -N
18	A7	38	Ø
19	A8	39	Ø2
20	A9	40	T4M

3.8.2 CASSETTE INTERFACE (CPU - BOARD CONN. 1)

1	+12V
2	L
3	L
4	L
5	-
6	WDA-N
7	BET-N
8	WCD-N
9	REV-N
10	FWD-N
11	RDC
12	RDA-N
13	CIP-N
14	WEN-N

3.8.3 KEYBOARD INTERFACE (CPU-BOARD CONNECTOR 2)

1	X9	11	Y0
2	X0	12	Y2
3	X4	13	Y3
4	X1	14	Y4
5	X3	15	Y7
6	X2	16	Y5
7	X7	17	Y1
8	X8	18	Y6
9	X6	19	+5V
10	X5	20	L

3.8.4 RESET SWITCH (CPU/3)

1 RESA-N
2
3 L

3.8.5 I/O CARTRIDGE INTERFACE (CPU CONNECTOR 4)

1	A	Ø	1	B	+5V
2	A	D0	2	B	D1
3	A	D2	3	B	D3
4	A	D4	4	B	D5
5	A	D6	5	B	D7
6	A	A0	6	B	A1
7	A	A2	7	B	A3
8	A	A4	8	B	A5
9	A	A6	9	B	A7
10	A	RD-N	10	B	RES-N
11	A	IORQ-N	11	B	M1
12	A	INT-N	12	B	L
13	A	BEEP 2	13	B	+12V
14	A	-12V	14	B	WR-N
15	A	L	15	B	L

3.8.6 ROM-CARTRIDGE INTERFACE (CPU CONNECTOR 5)

1	A	NMI-N	1	B	+5V
2	A	DM 0	2	B	DM1
3	A	DM 2	3	B	DM3
4	A	DM 4	4	B	DM5
5	A	DM 6	5	B	DM7
6	A	A0	6	B	A1
7	A	A2	7	B	A3
8	A	A4	8	B	A5
9	A	A6	9	B	A7
10	A	A8	10	B	A9
11	A	A10	11	B	A11
12	A	A12	12	B	CARS1-N
13	A	CARS 2-N	13	B	---
14	A	--	14	B	MRQ-N
15	A	L	15	B	L

3.8.7 PRINTER INTERFACE (CPU CONNECTOR 7)

1 NC
2 PRI (RCD)
3 PRO (TMD)
4 NC
5 HIGH (LOW SELECTION WITH STRAP E)
6 HIGH (LOW SELECTION WITH STRAP F)
7 L
20 READY (PRINTER READY)

Signal levels in accordance with V28/RS232-C (+12/-12)

3.8.8 HF - MODULATOR INTERFACE (CPU CONNECTOR 8)

1	L
2	+5V (FILTERED)
3	BURSTFL(AG)-N
4	B (BLUE)
5	BURSTFL
6	PAL-FF
7	G (GREEN)
8	Y (MONOCHROME)
9	+12V (FILTERED)
10	R (RED)
11	NC
12	SYNC (POSITIVE)
13	BEEP (SOUND)
14	NC
15	L
16	HF-OUTPUT
17	L

3.8.9 RGB INTERFACE (CPU CONNECTOR 11)

1	GREEN
2	SYNC
3	L
4	RED
5	BLUE
6	BEEP

3.8.10 MONITOR INTERFACE (VIDEO PCB CONNECTOR 3 - MONITOR)

CONNECTOR 3 VIDEO PCB	CONNECTOR MONITOR	SIGNAL
1	1	L
2	1	L
3	9	VERT. SYNC
4	8	VIDEO
5	6	HORZ. SYNC.
	7	+12V
	10	GND, LOGIC
	5	GND, PROT
	8	EXT. BRIGHTNESS
	10	EXT. BRIGHTNESS

3.8.11 VIDEO BOARD TO EXTENSION BOARD

1	L	21	AU10
2	L	22	AU11
3	DU0	23	AU12
4	DU1	24	AU13
5	DU2	25	AU14
6	DU3	26	RAMSU
7	DU4	27	MREQU-N
8	DU5	28	RDU-N
9	DU6	29	INT-N
10	DU7	30	WRU-N
11	AU0	31	IORQU-N
12	AU1	32	WAIT-N
13	AU2	33	M1U
14	AU3	34	RES-N
15	AU4	35	LOCK-N
16	AU5	36	RFSHU-N
17	AU6	37	DEW/R2425-N
18	AU7	38	ØU
19	AU8	39	Ø2
20	AU9	40	NC

3.8.12 FLOPPY INTERFACE

1	L	18	DIRECTION
2	NC	19	L
3	L	20	STEP-N
4	NC	21	L
5	L	22	WRITE DATA-N
6	NC	23	L
7	L	24	WRGATE-N
8	INDEX-N	25	L
9	L	26	TRACK00-N
10	DRISEL 1-N	27	L
11	L	28	WRPROT-N
12	DRISEL 2-N	29	L
13	L	30	READ DATA-N
14	DRISEL 3	31	L
15	L	32	HEADSEL-N
16	MOTORON-N	33	L
17	L	34	NC

3.9 KEY TO DIAGRAMS

3.9.1 LOGIC SYMBOLS

The logic symbols used on the diagrams are according to IEC STANDARDS (concern standardization 4T-D 1164-02)
Figure 3.16 is an example to illustrate the main notation rules.

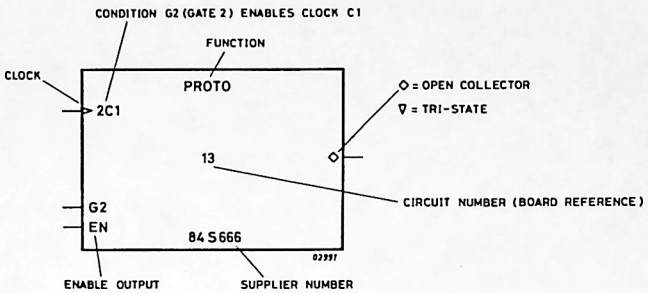

Figure 3.16 LOGIC SYMBOLS

3.9.2 LOGIC CIRCUITS

74 LS00A	QUAD 2 - INPUT NAND	
74 LS02A	QUAD 2 - INPPUT NOR	SIGNETICS
03	QUAD 2 - INPUT NAND, OPEN COLL.	"
04A	HEX INVERTER	"
08A	QUAD 2 - INPUT AND	"
10	TRIPLE 3 - INPUT NAND	"
11	TRIPLE 3 - INPUT AND	
12A	TRIPLE 3 - INPUT NAND, OPEN COLL.	
16	HEX INVERTER/BUFFER	
27	TRIPLE 3 - INPUT NOR	
32A	QUAD 2 - INPUT OR	
38	QUAD 2 - INPUT NAND, OPEN COLL.	
74A	DUAL D -TYPE FLIP-FLOP	
85	4- BIT COMPARATOR	
86A	QUAD 2 - INPUT EXCLUSIVE - OR	
107A	DUAL JK FLIP-FLOP	
109	DUAL JK FLIP-FLOP (POS. EDGE TRIGGERED)	
123	RETRIGGERABLE MONO STABLE MULTIVIBRATOR	
132	QUAD 2 - INPUT NAND, SCHMITT TRIGGER	
138B	3 - TO - 8 LINE DECODER	
139N	DUAL 2 - TO 4 LINE DECODER	
145B	BCD - TO - DECIMAL DECODER/DRIVER	
153N	DUAL 4 TO - LINE MULTIPLEXER	
157B	QUAD 2 - TO - 1 LINE MULTIPLEXER	
161B	4 - BIT BINARY COUNTER	
163B	4 - BIT BINARY COUNTER	
166	8 - BIT SERIAL/PARALLEL	
168N	4 - BIT 4P/DOWN SYNCHR. COUNTER	
174	HEX D-TYPE FF	
175B	QAUD D	FLIP-FLOP
193B	4 - BIT SYNCHR. BINARY UP/DOWN COUNTER	"
273B	OCTAL D - FLIP-FLOP	"
295	4 - BIT RIGHT/LEFT SHIFT REGISTER	"

367N	HEX BUFFER/DRIVER	SIGNETICS
INT3216	4 BIT BIDIRECTIONAL BUS DRIVER	INTEL
DM81LS97	TRI - STATE OCTAL BUFFERS	
DP8304	TRI - STATE OCTAL TRANSCEIVER	NATIONAL
MC1488	QUAD LINE DRIVER	MOTOROLA
MC1489	QUAD LINE RECEIVER	MOTOROLA
HEF4013BP	DUAL D-FF	SIGNETICS
HEF4022BP	DIVIDE BY 8 JONNION COUNTER	"
HEF40097BP	3-STATE HEX-BUFFER	"
MK1007 P	4 x 80 BIT SHIFT REGISTER	MOSTEK
HM 472114/4	1K4 STATIC RAM	HARRIS
MK 4116-4	16K1 DYNAMIC RAM	MOSTEK
82S123N	32 x 8 BIPOLAR ROM	SIGNETICS
82S129N	256 x 4 BIPOLAR ROM	"
LM1886	VIDEO MATRIX D TO A	NATIONAL
LM1889	VIDEO MODULATOR	NATIONAL
SAA5020	TELETEX TIMING CHAIN	PHILIPS
SAA505X	TROM-CHARACTER GENERATOR	PHILIPS
µPD765	FLOPPY CONTROLLER	NEC
Z80-CTC	COUNTER/TIMER CIRCUIT	ZILOG
Z80-CPU	MICROPROCESSOR	ZILOG

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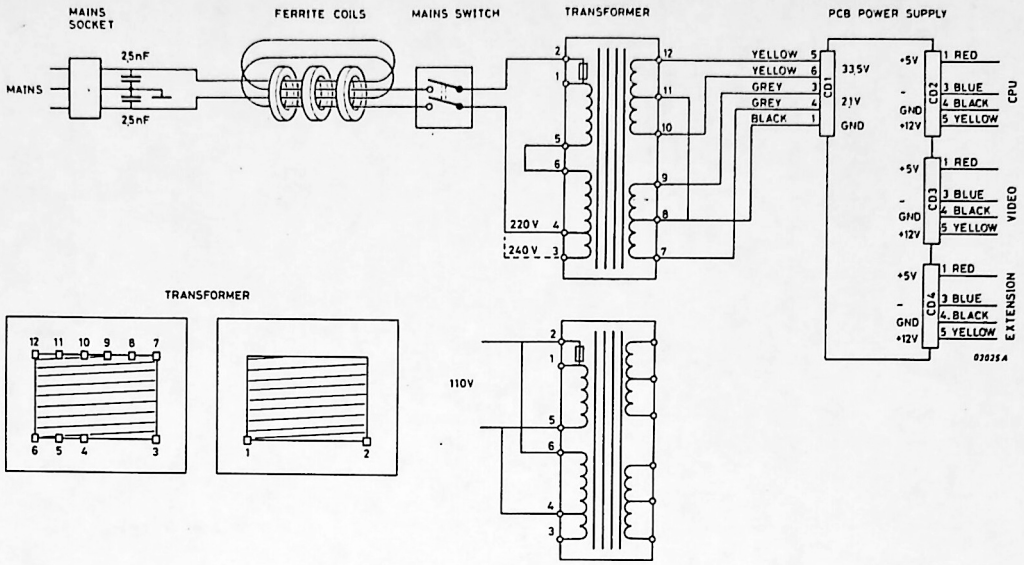


Figure 4.1 POWER SUPPLY DISTRIBUTION BASIC CABINET

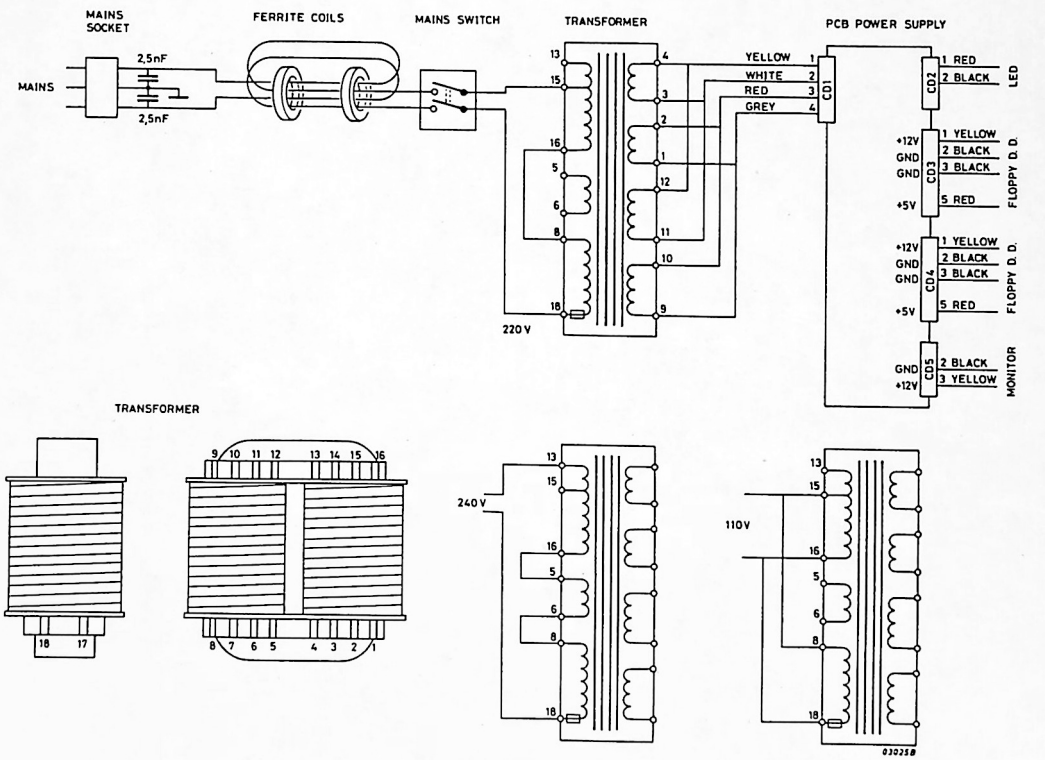


Figure 4.2 POWER SUPPLY DISTRIBUTION MONITOR CABINET

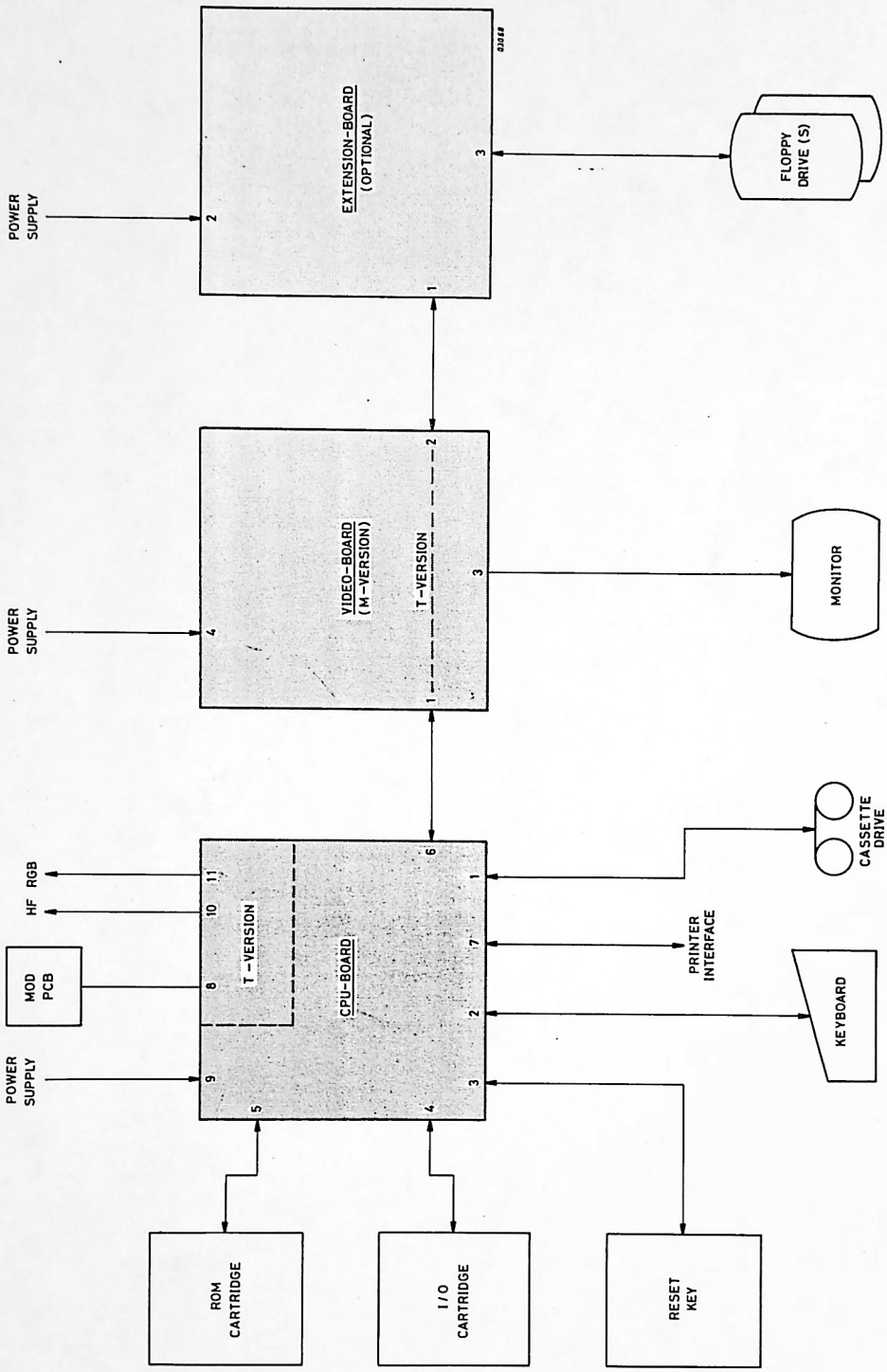


Figure 4.3 INTERCONNECTION DIAGRAM

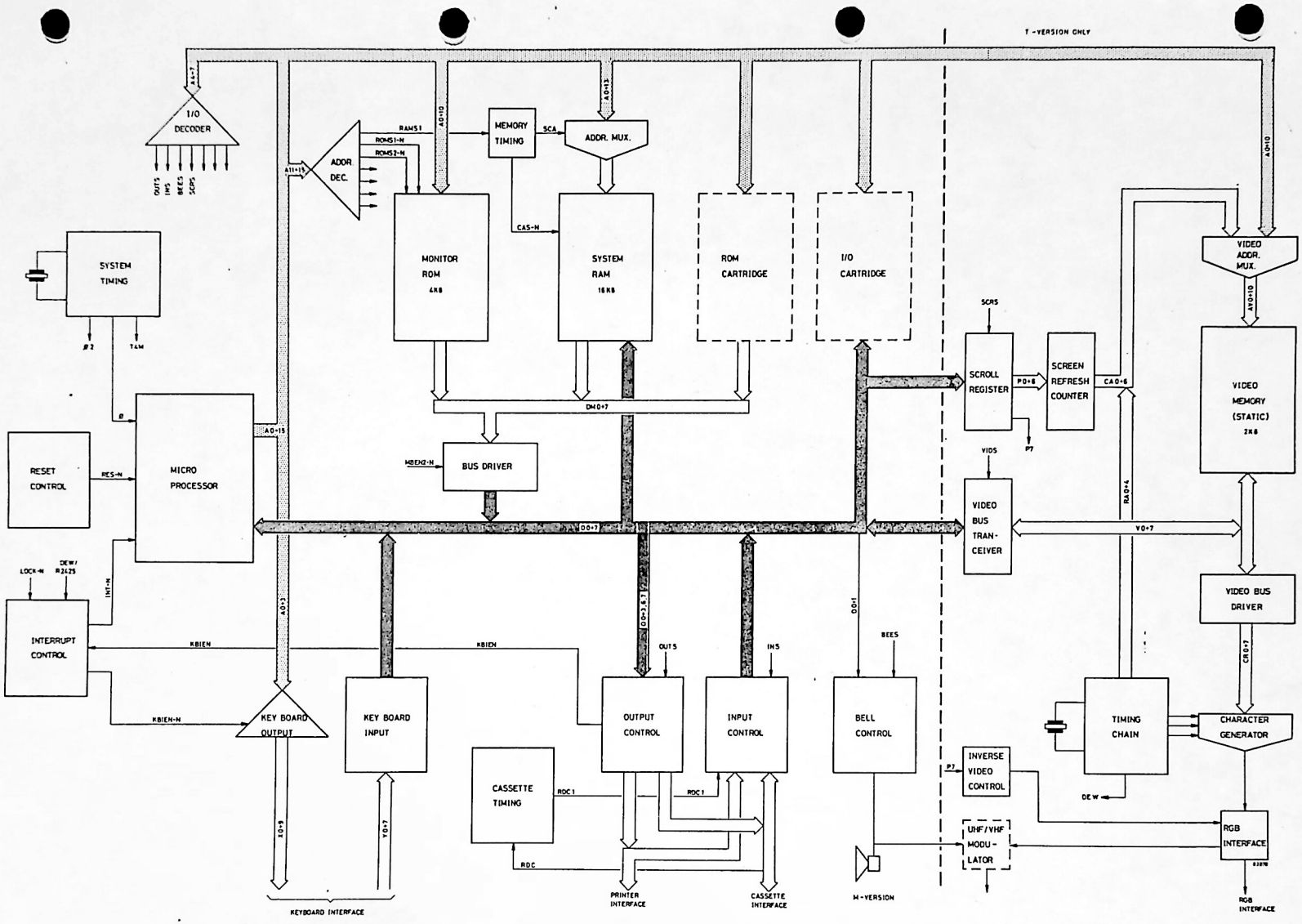


Figure 4.4 BLOCK DIAGRAM CPU-BOARD

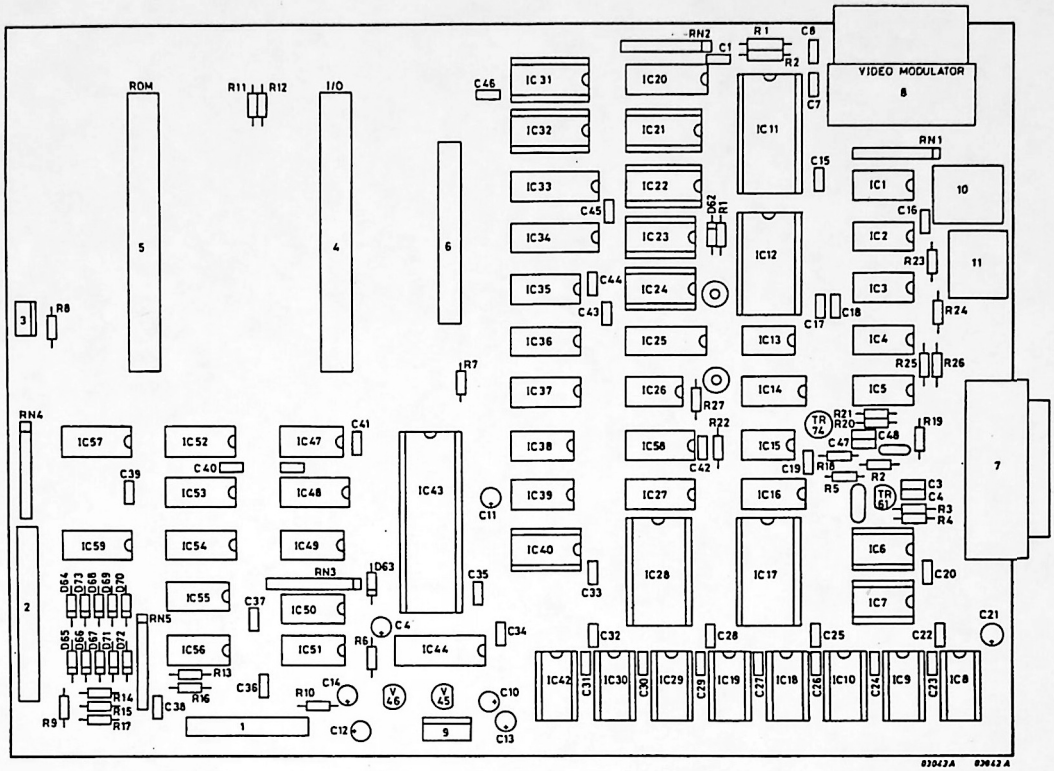


Figure 4.5 COMPONENT LAYOUT CPU-BOARD

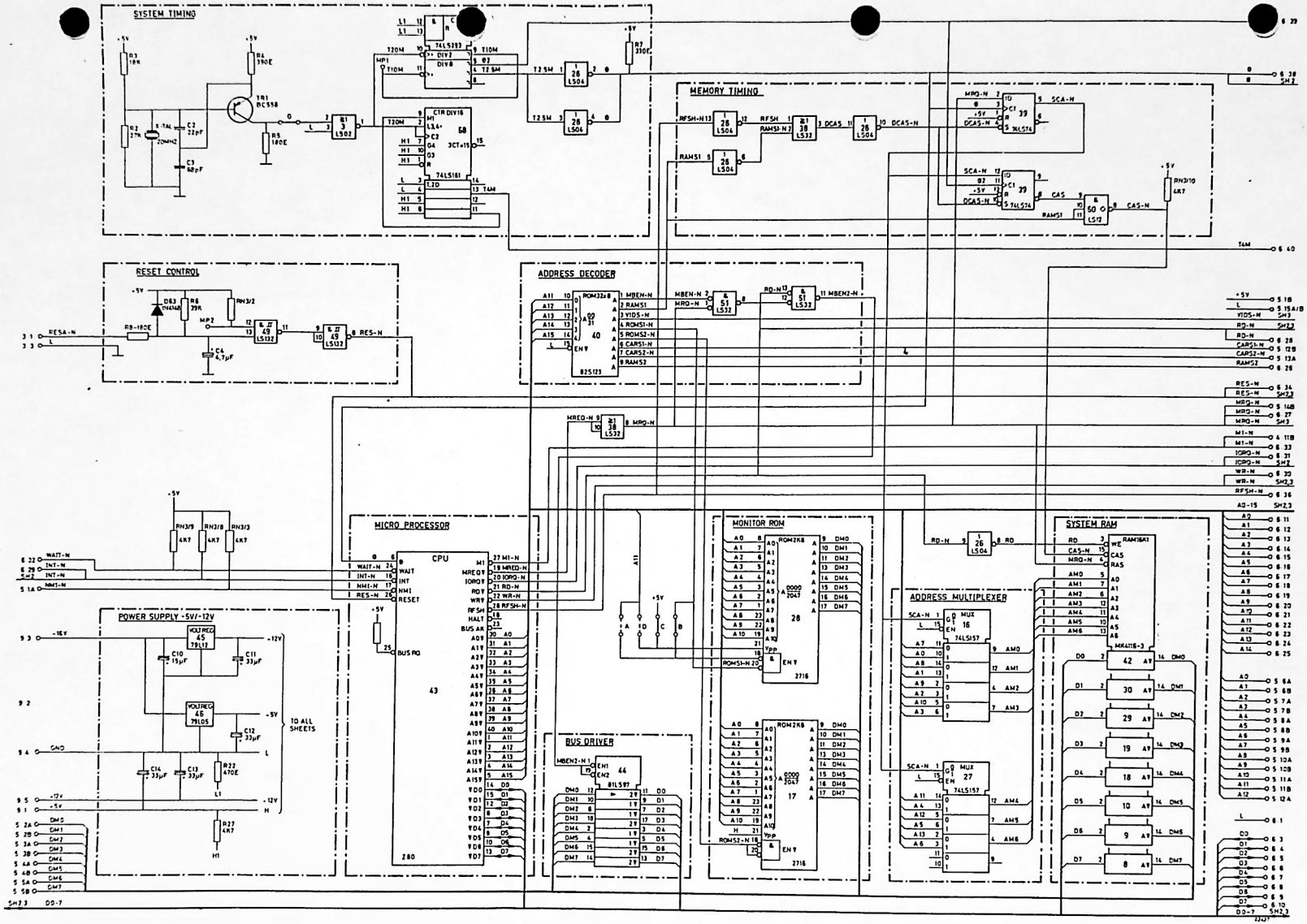


Figure 4.6.1 CPU-BOARD (CPU/MEMORY) SHEET 1

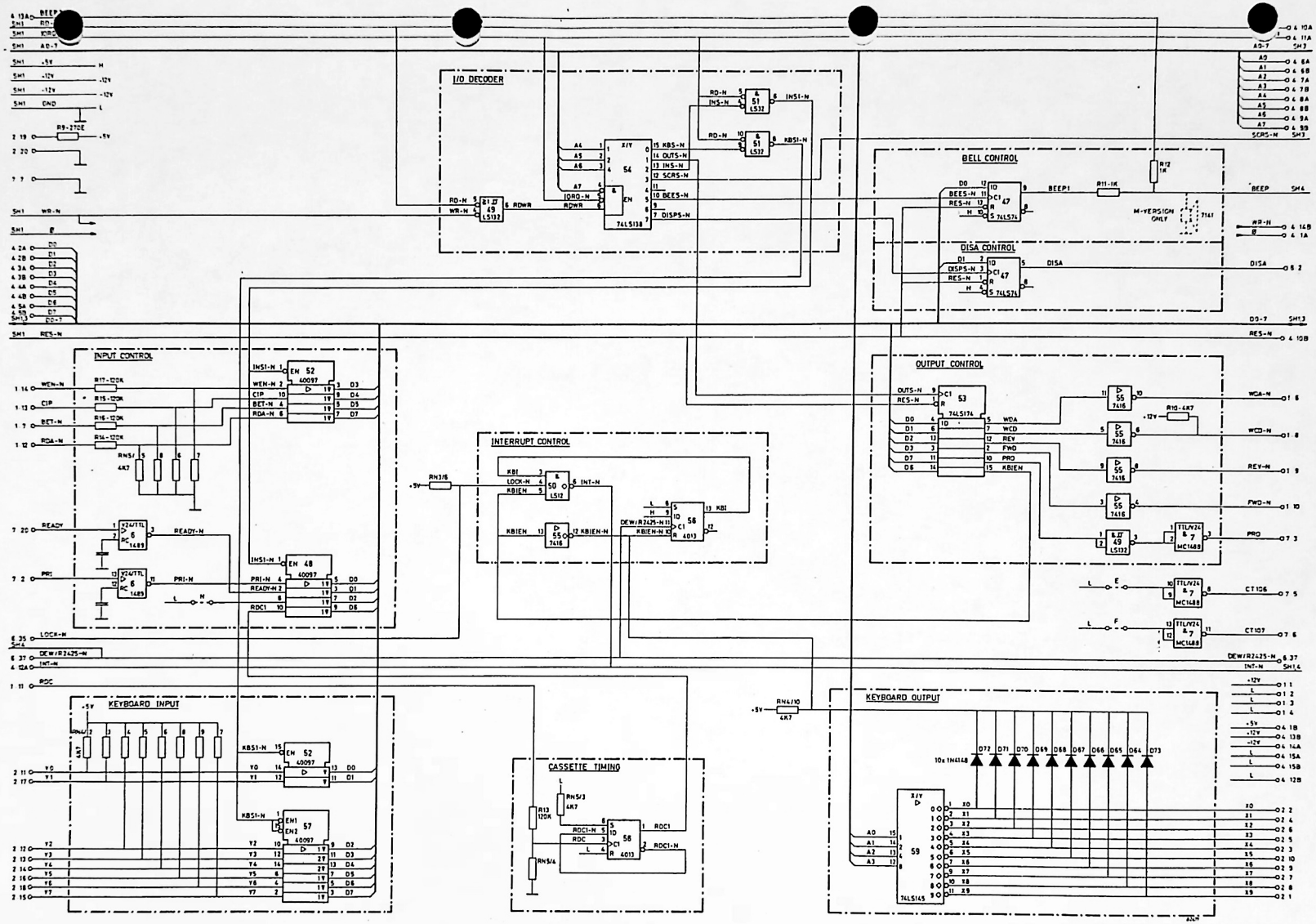


Figure 4.6.2 CPU-BOARD (I/O CONTROL)
SHEET 2

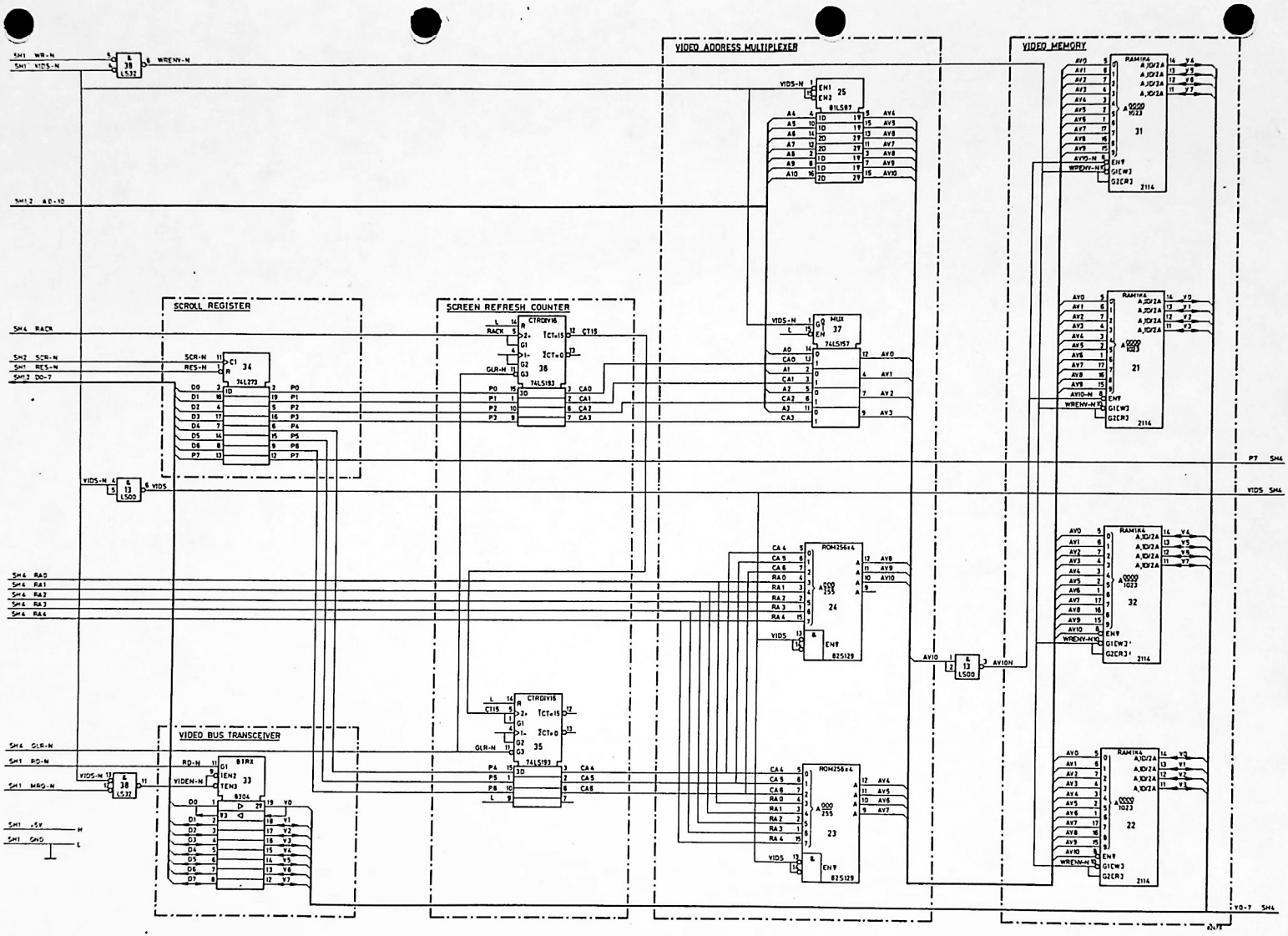


Figure 4.6.3 CPU-BOARD (VIDEO MEMORY)
SHEET 3

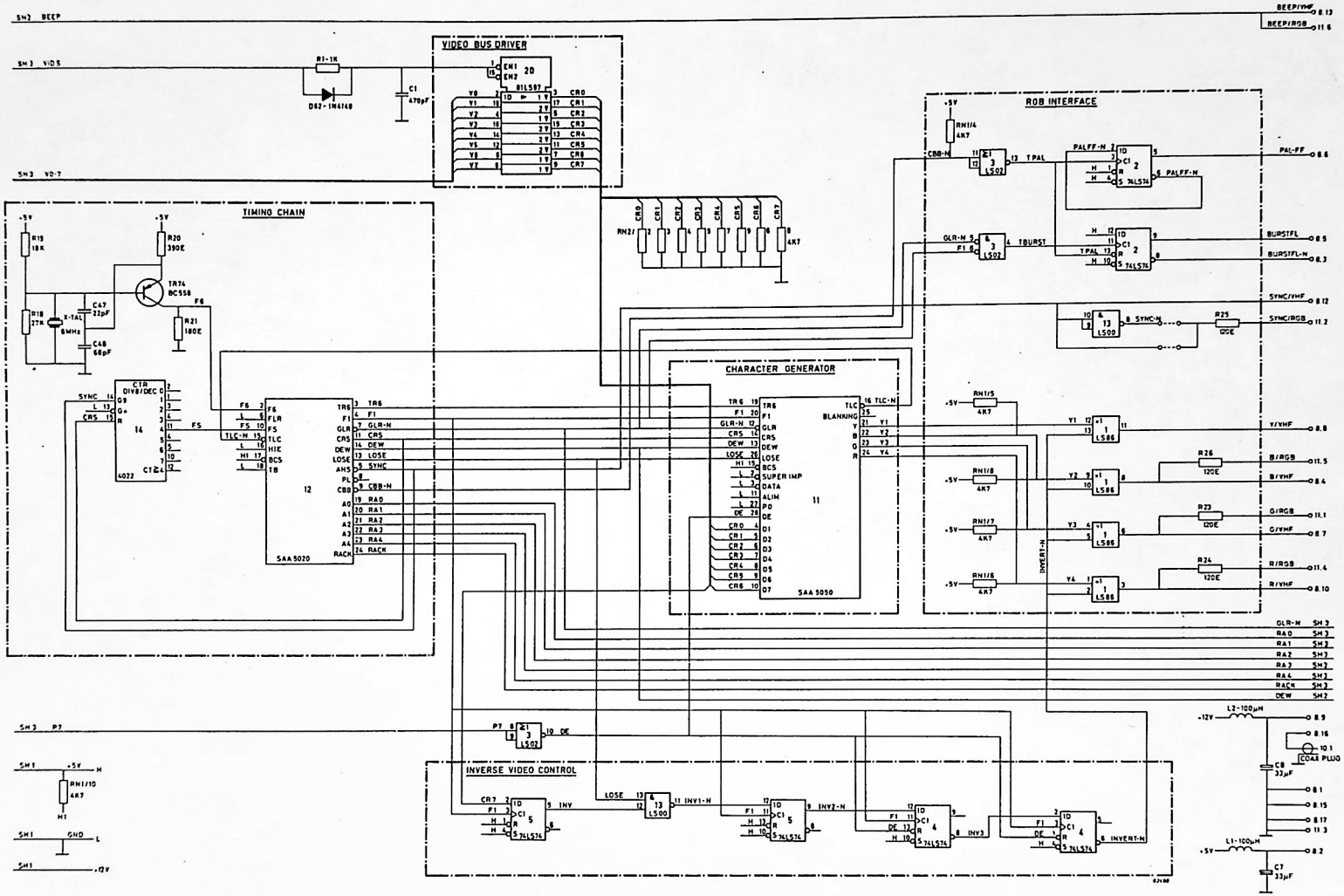


Figure 4.6.4 CPU-BOARD (VIDEO GENERATION)
SHEET 4

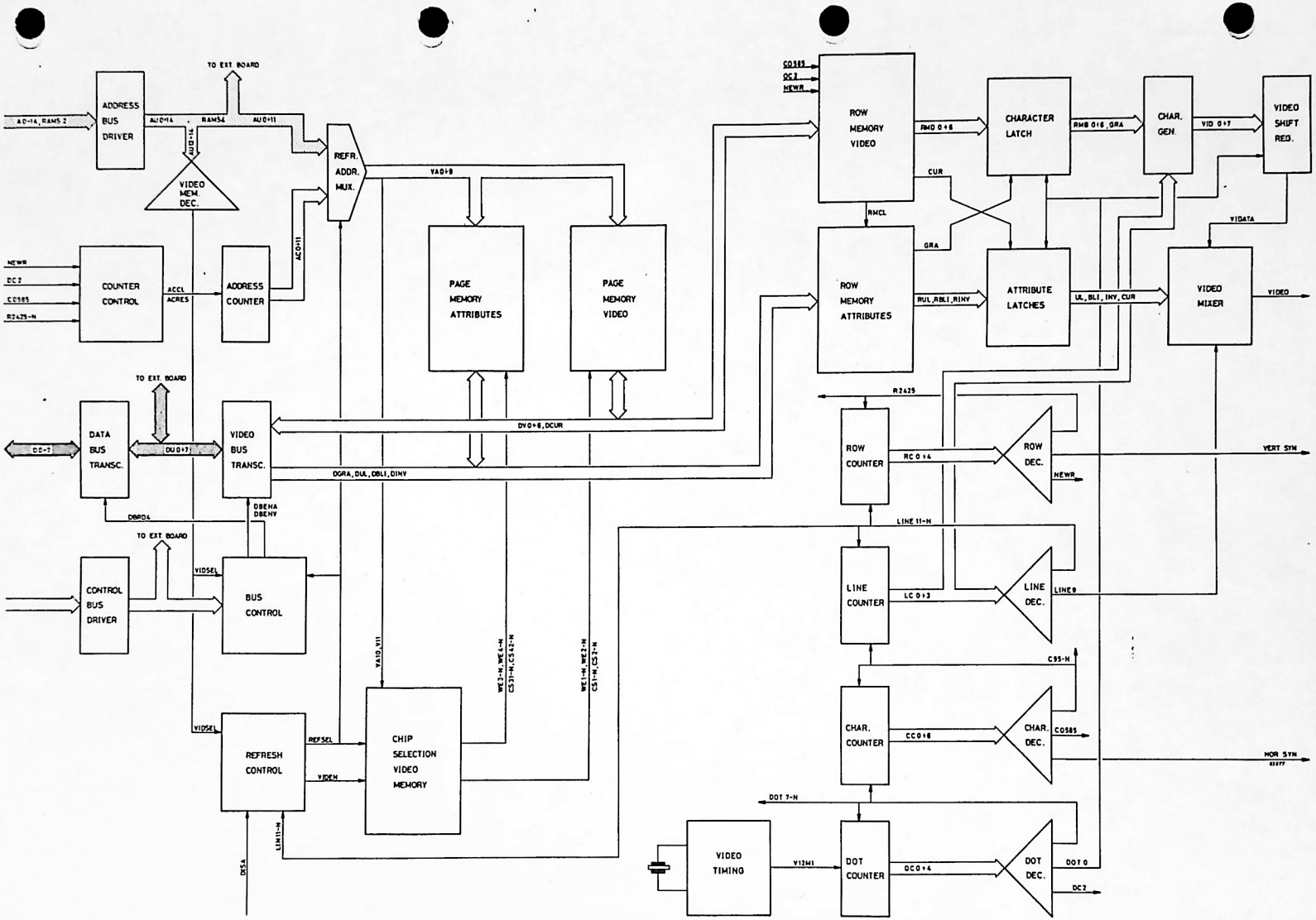


Figure 4.7 BLOCK DIAGRAM VIDEO BOARD

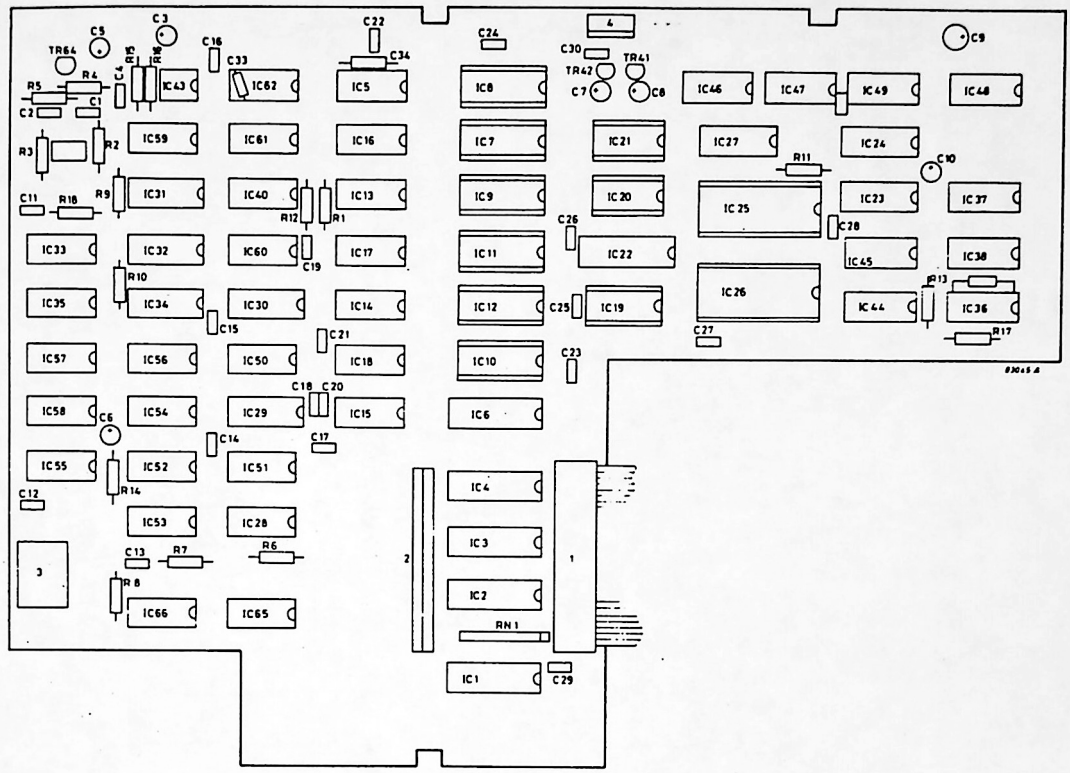


Figure 4.8 COMPONENT LAYOUT VIDEO BOARD

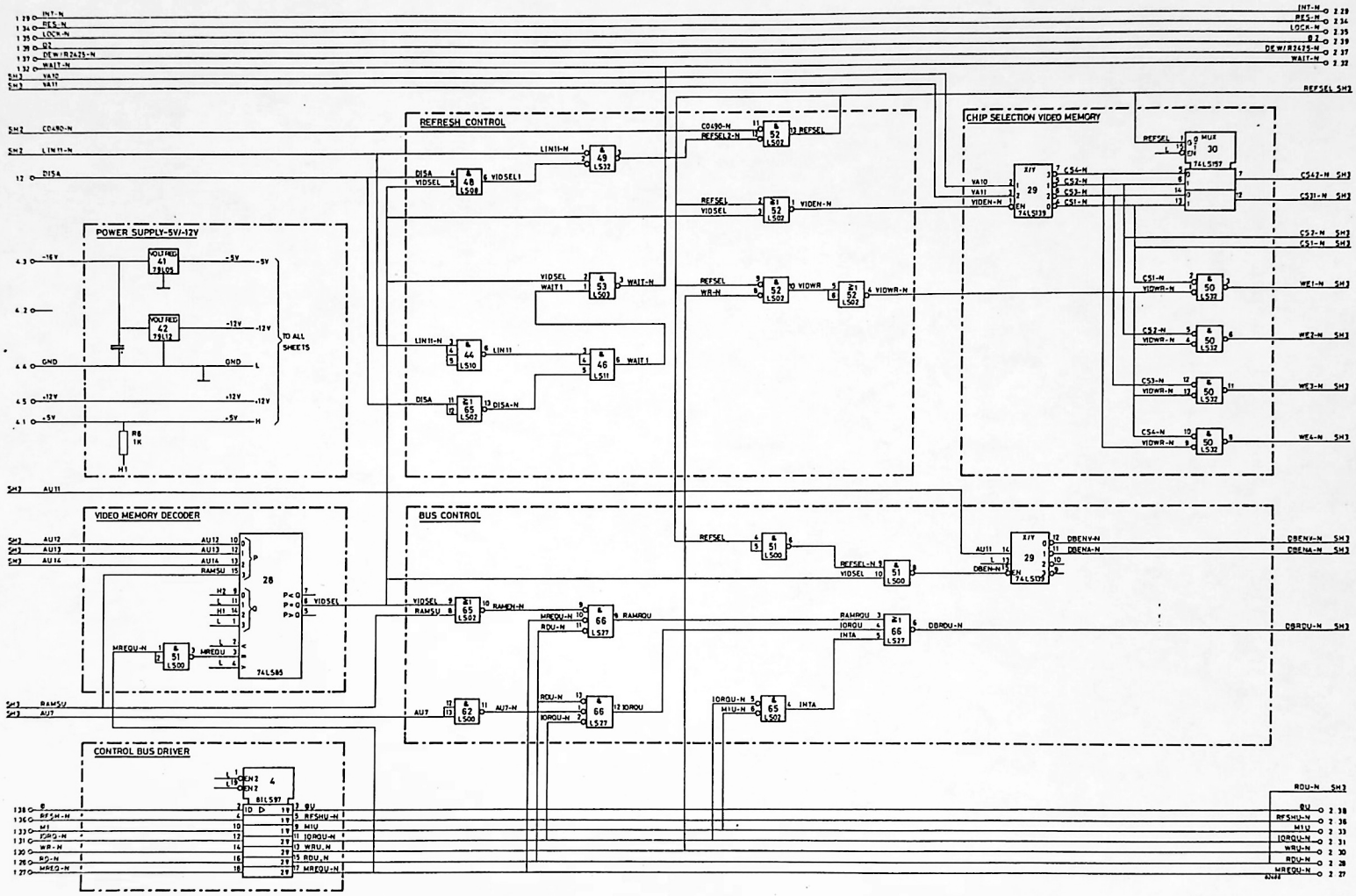


Figure 4.9.1 VIDEO BOARD (BUS CONTROL)
SHEET 1

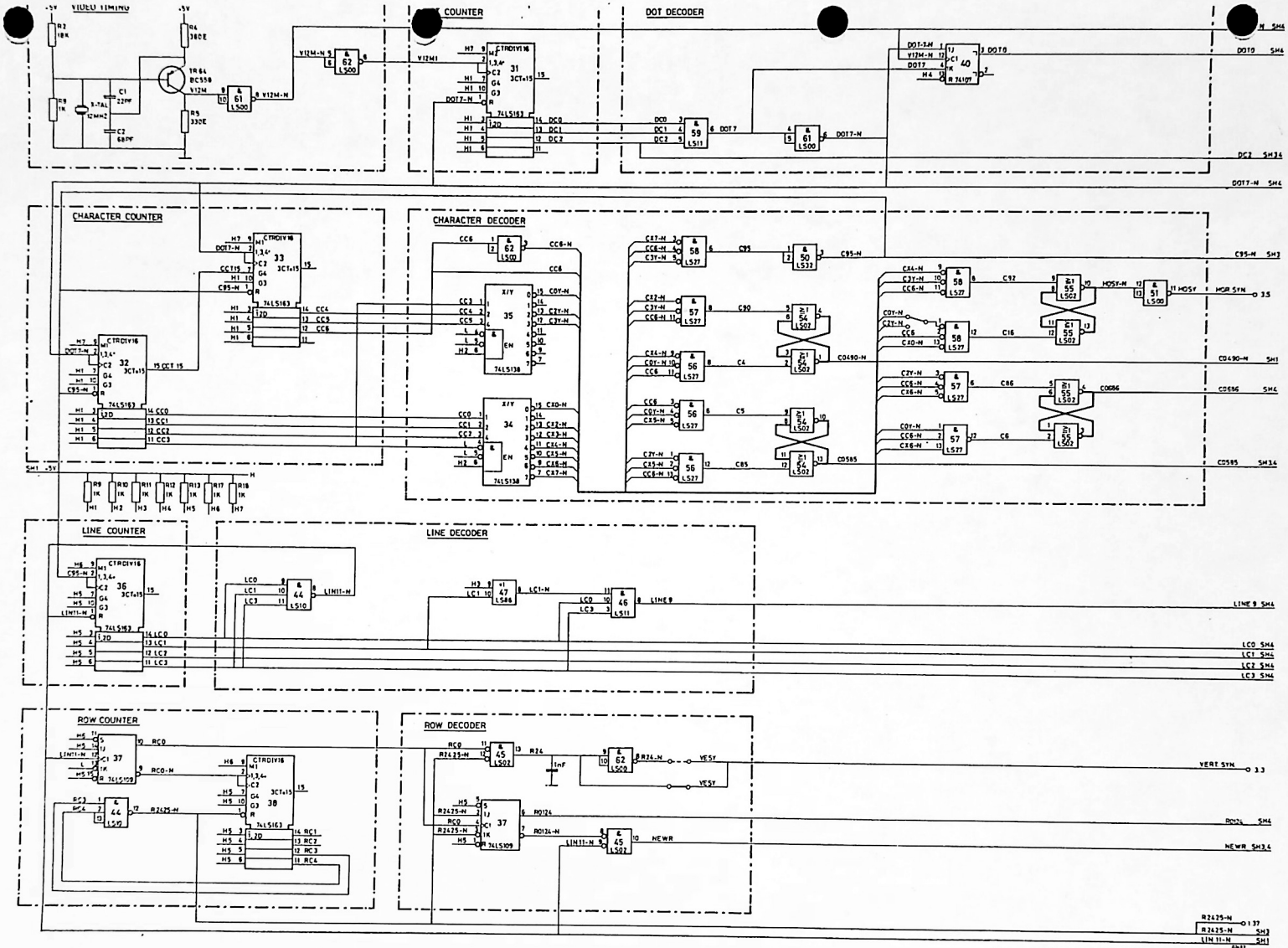


Figure 4.9.2 VIDEO BOARD (VIDEO TIMING)
SHEET 2

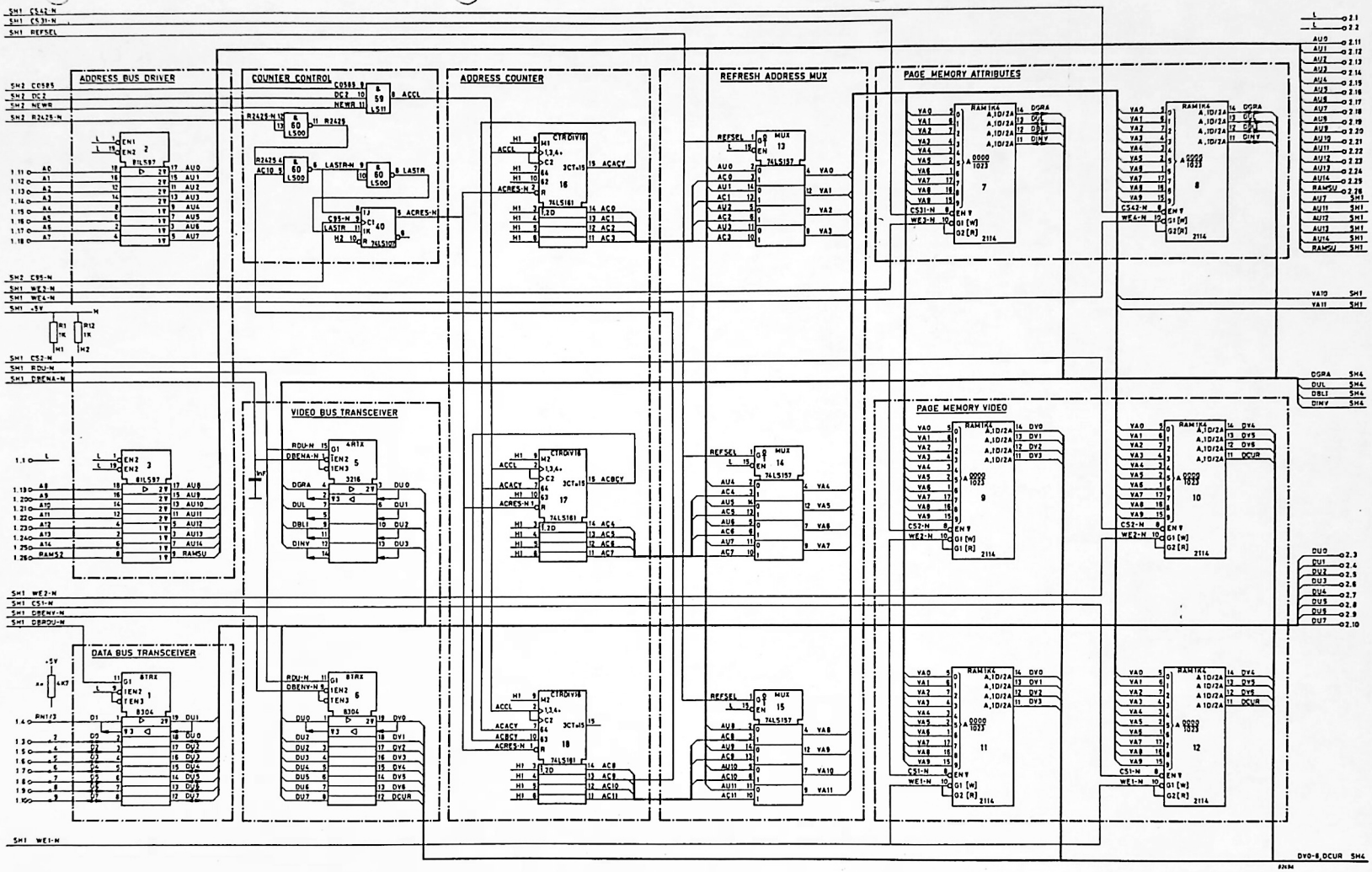


Figure 4.9.3 VIDEO BOARD (VIDEO MEMORY)
SHEET 3

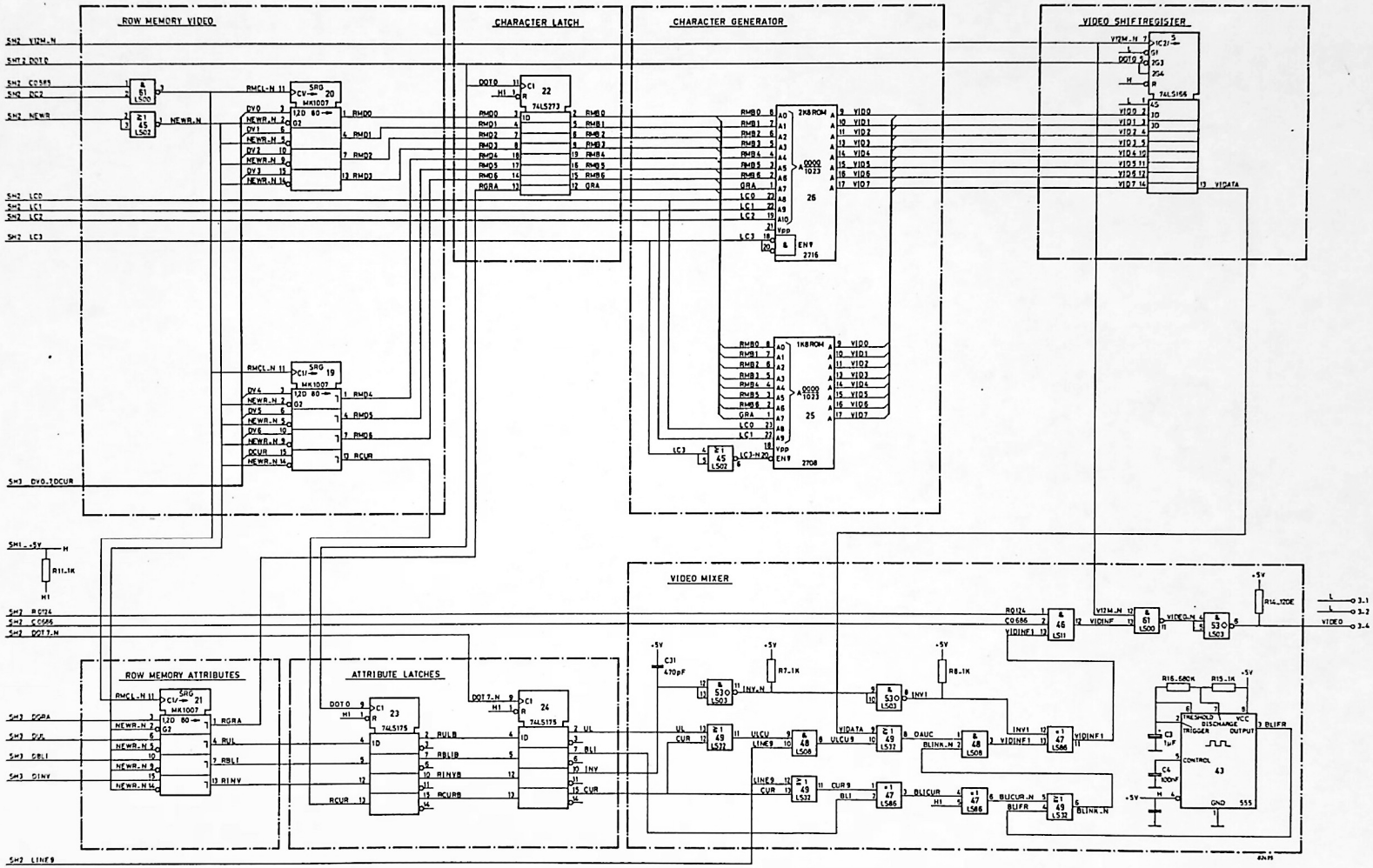


Figure 4.9.4 VIDEO BOARD (VIDEO GENERATION)
SHEET 4

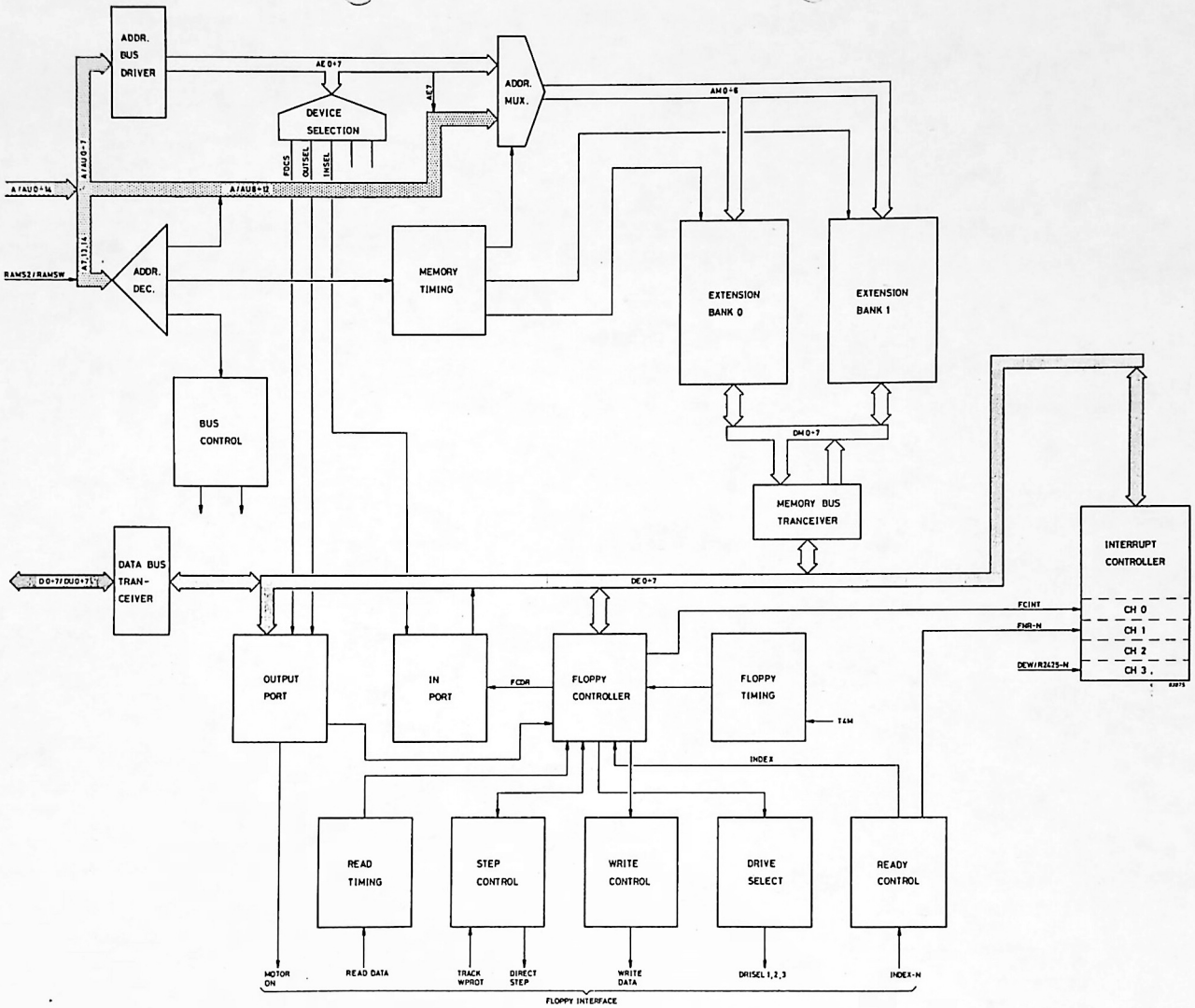


Figure 4.10 BLOCK DIAGRAM EXTENSION BOARD

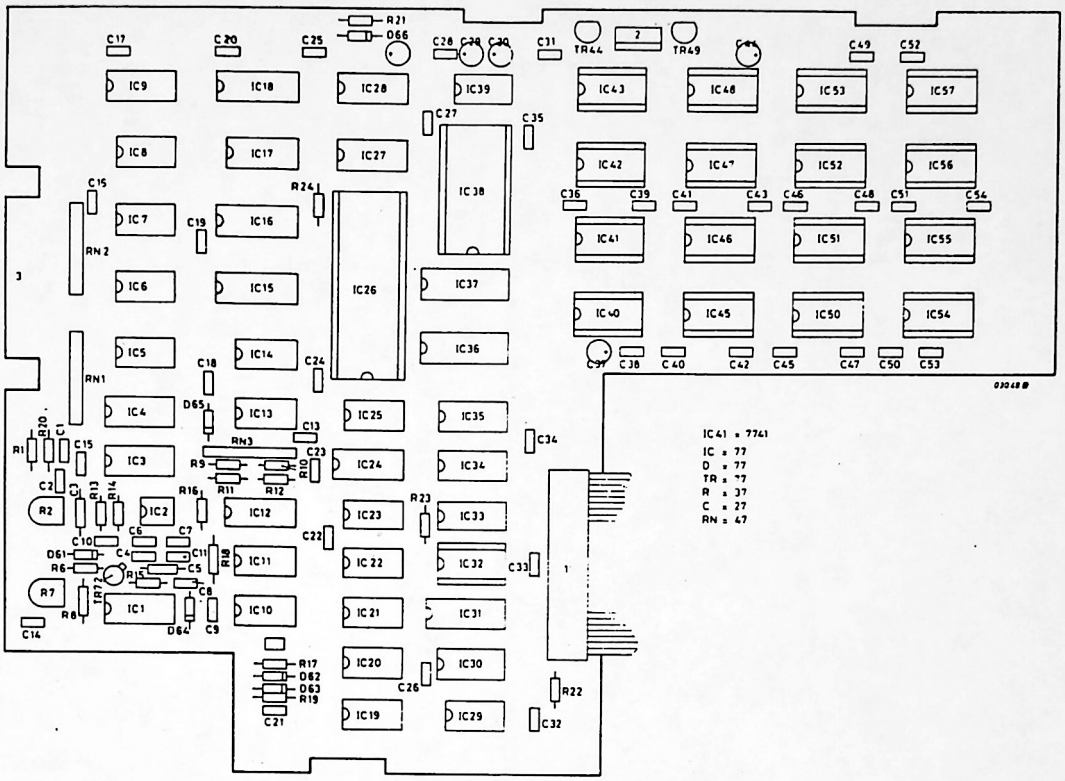


Figure 4.11 COMPONENT LAYOUT EXTENSION BOARD

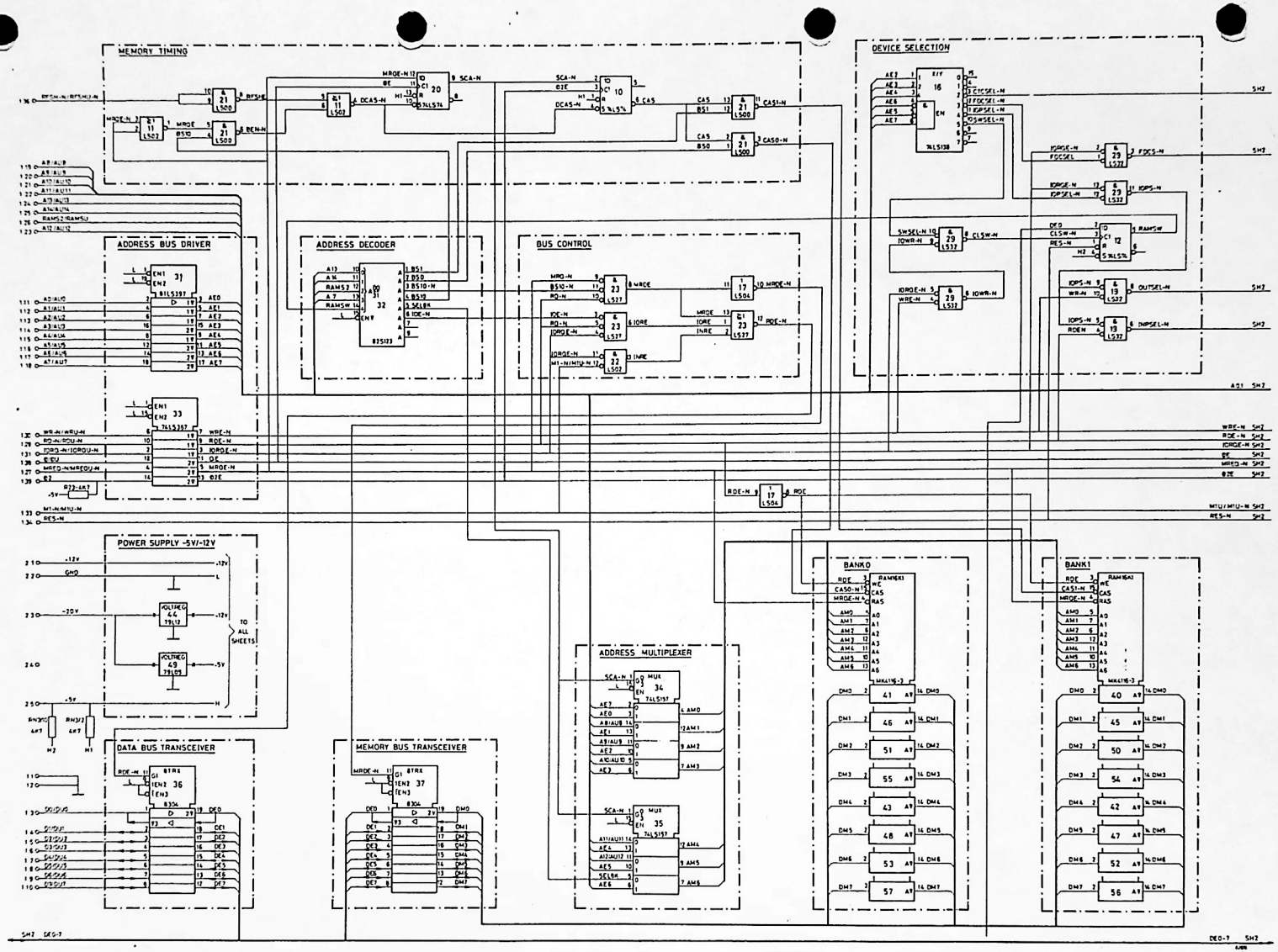


Figure 4.12.1 EXTENSION BOARD (MEMORY EXTENSION) SHEET 1

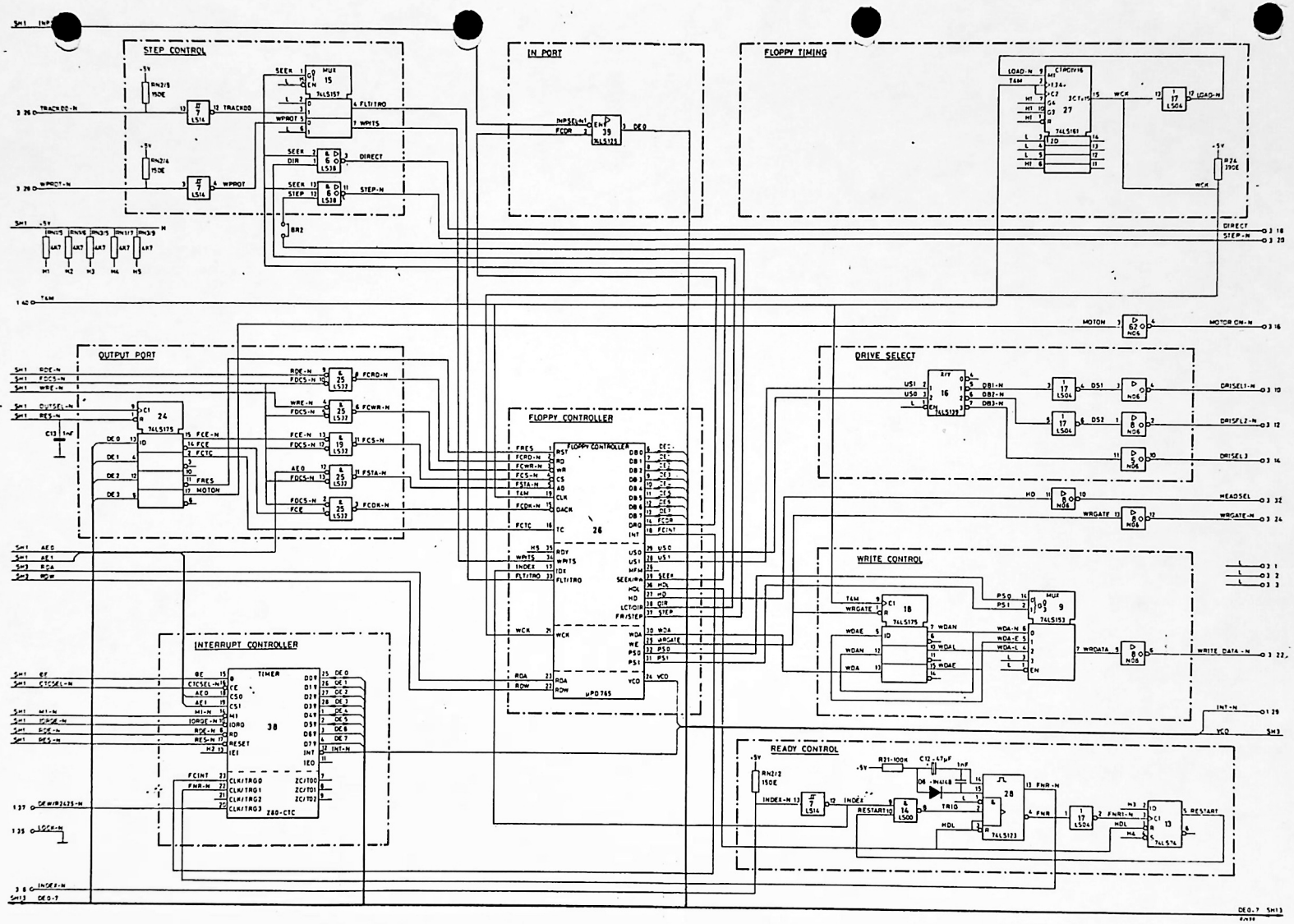


Figure 4.12.2 EXTENSION BOARD (FLOPPY CONTROL) SHEET 2

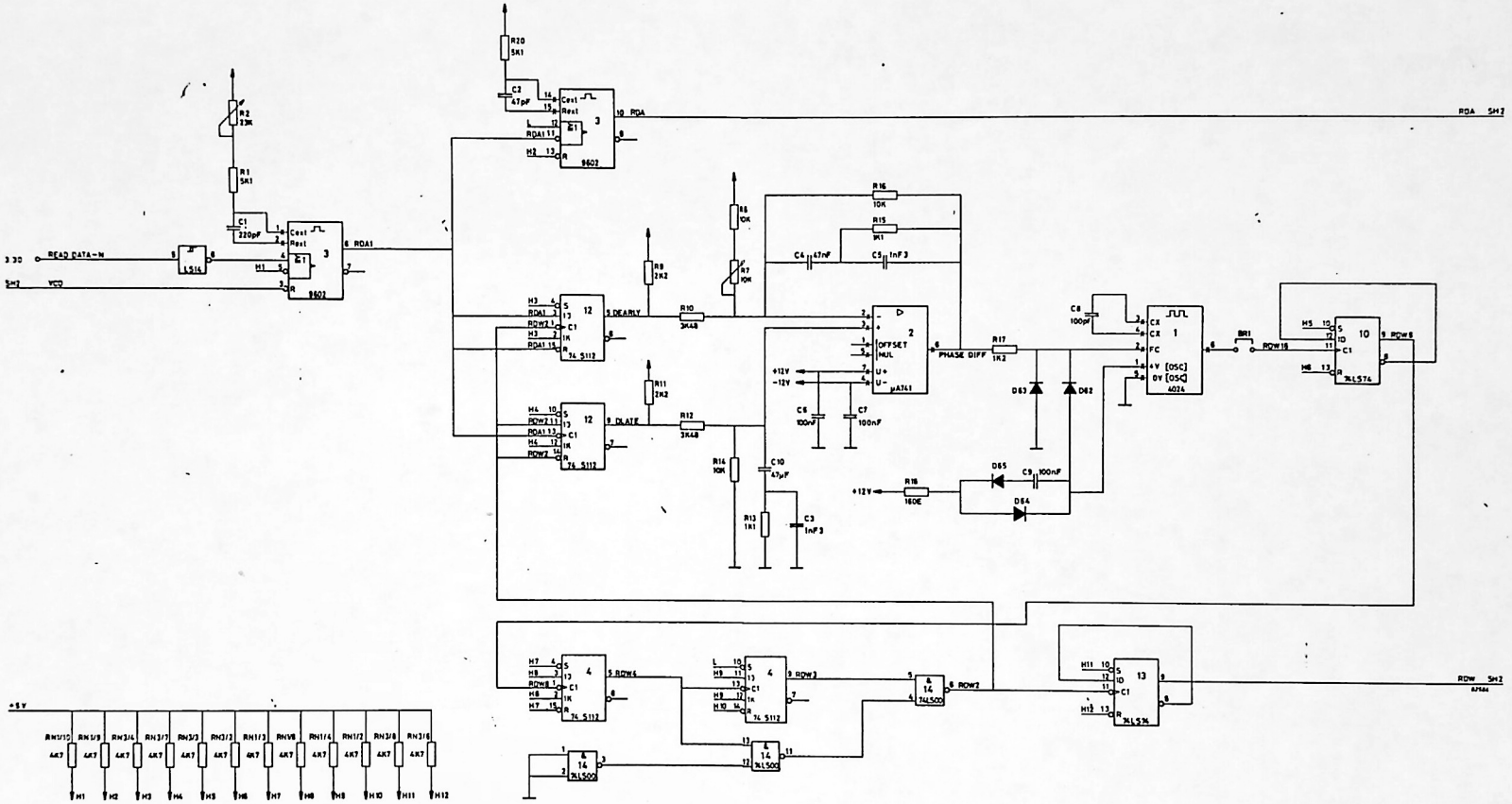


Figure 4.12.3 EXTENSION BOARD (READ TIMING) SHEET 3

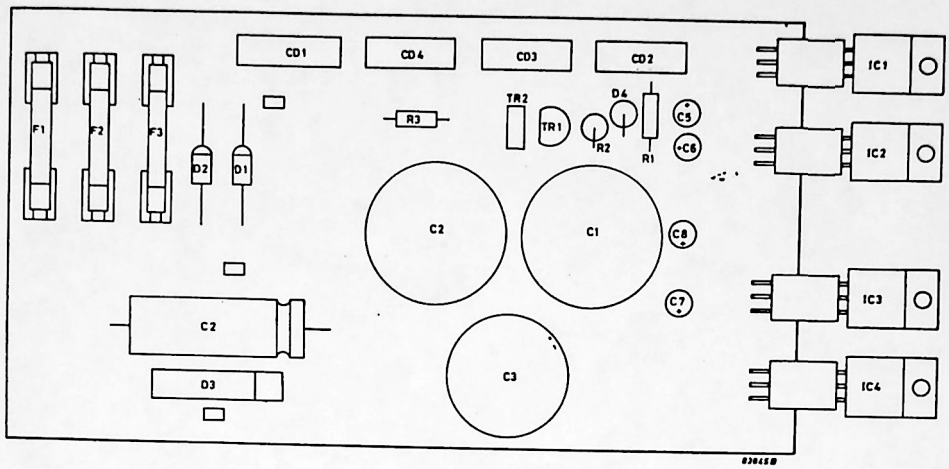


Figure 4.13 COMPONENT LAYOUT POWER SUPPLY BASIC CABINET

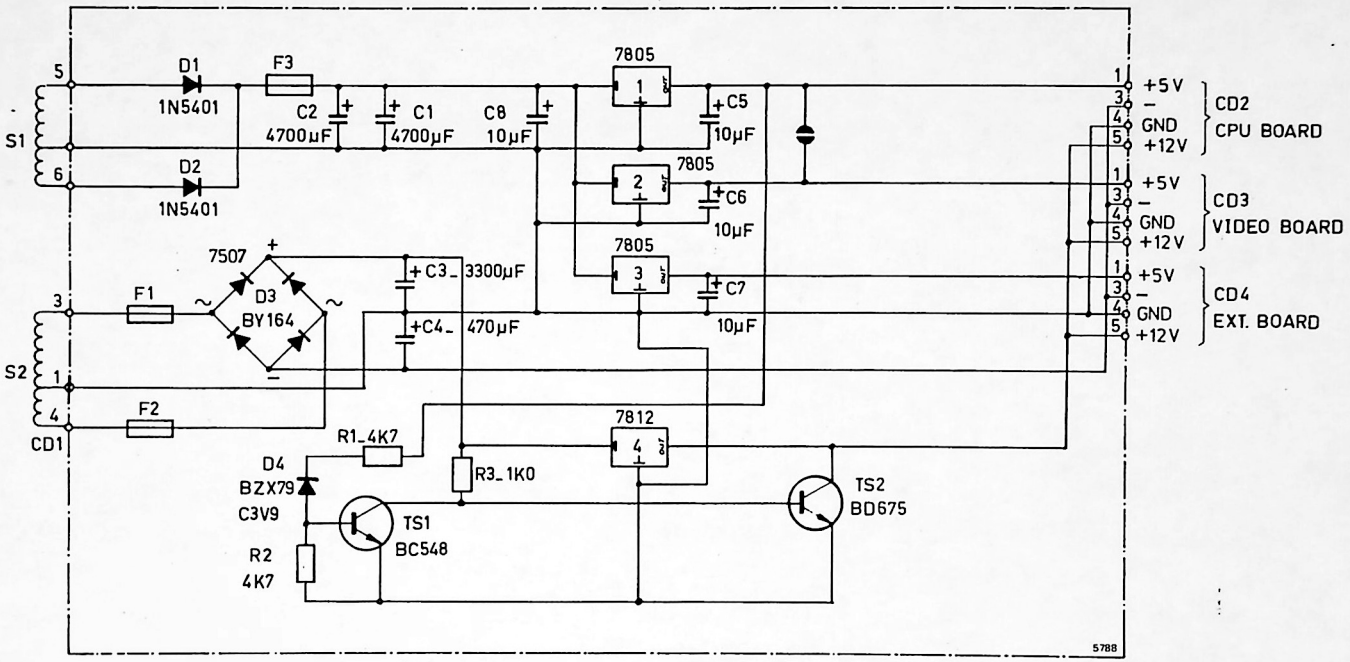
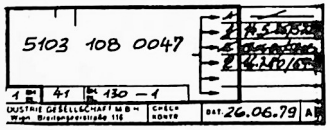


Figure 4.14 POWER SUPPLY BASIC CABINET



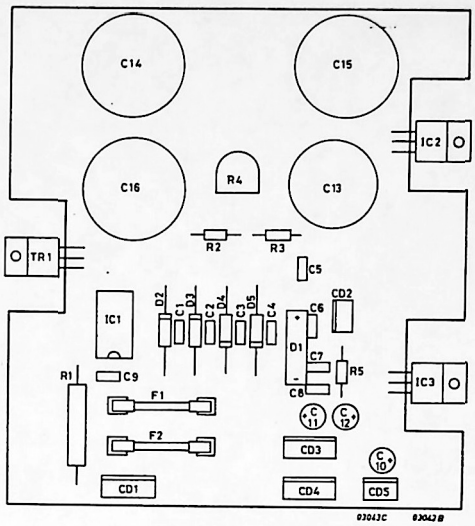


Figure 4.15 COMPONENT LAYOUT POWER SUPPLY MONITOR CABINET

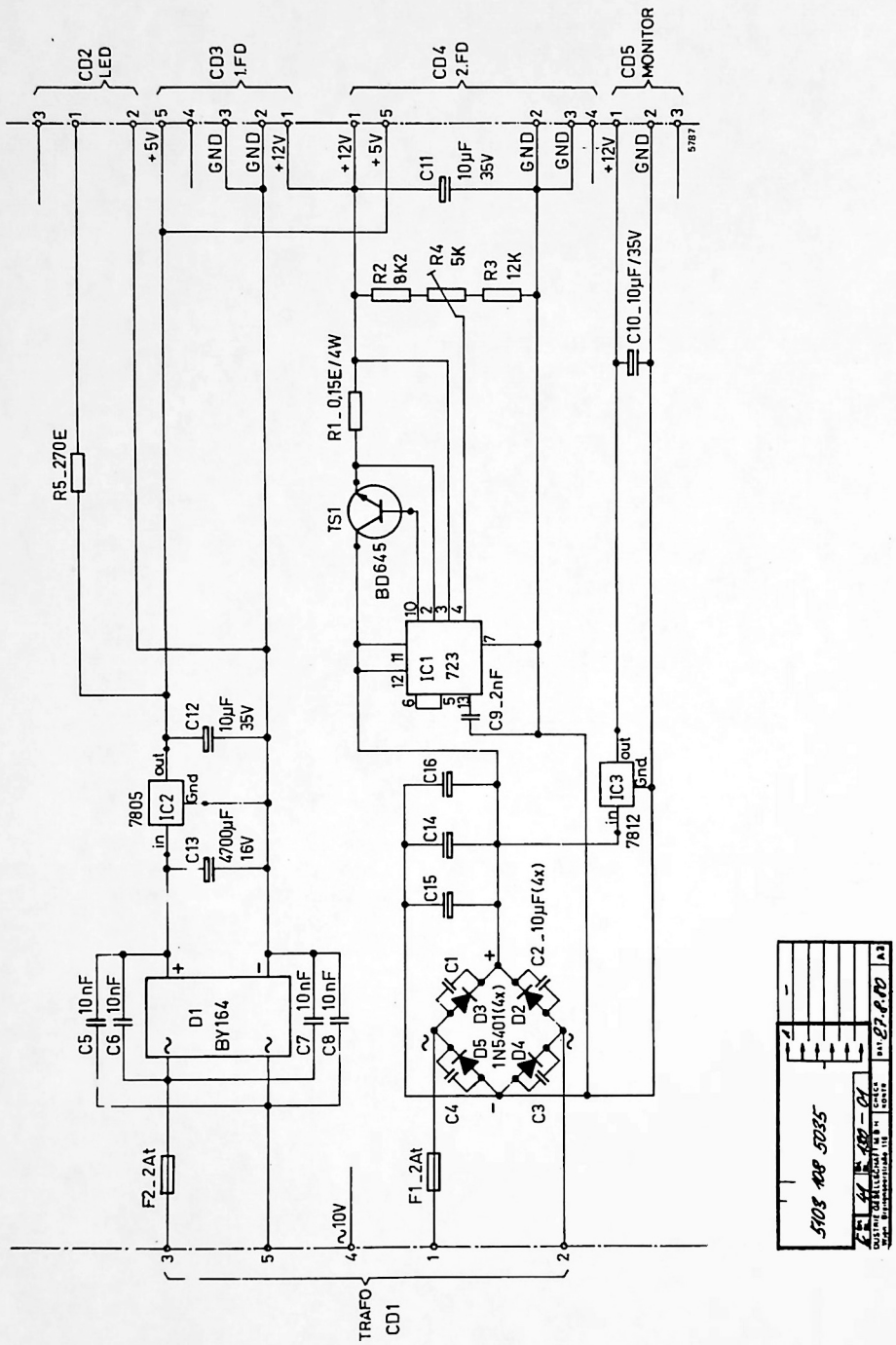


Figure 4.16 POWER SUPPLY MONITOR CABINET

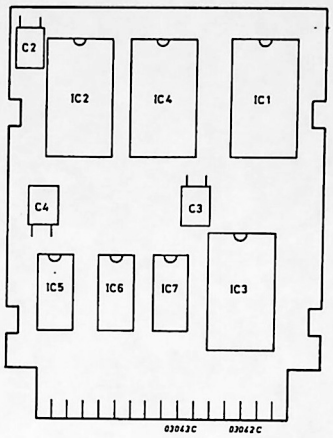


Figure 4.17 COMPONENT LAYOUT ROM-CARTRIDGE

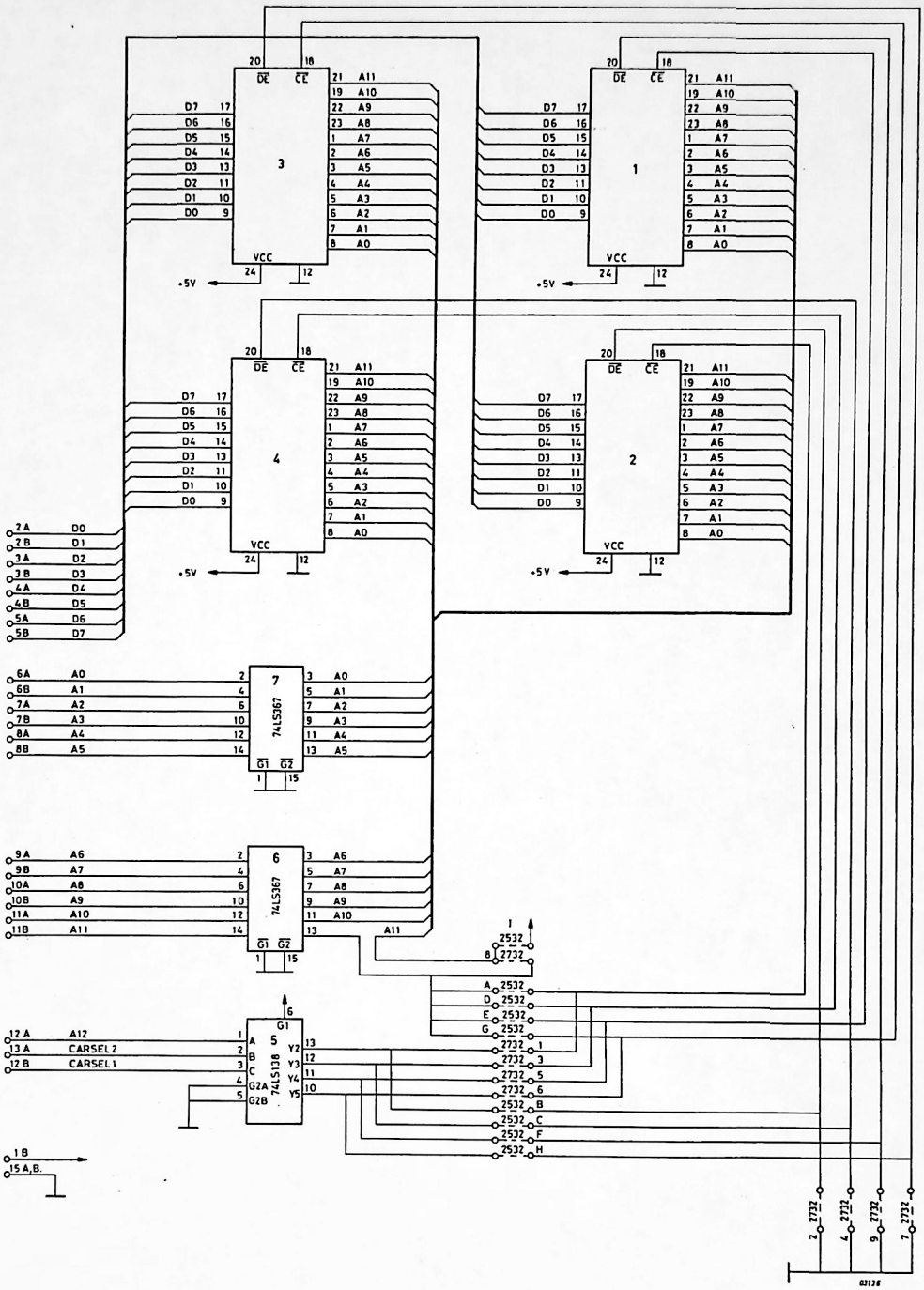


Figure 4.18 LOGIC DIAGRAM ROM-CARTRIDGE

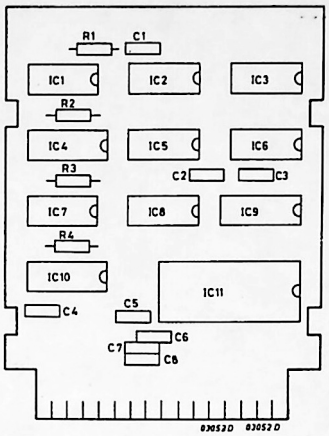


Figure 4.19 COMPONENT LAYOUT VIEWDATA INTERFACE

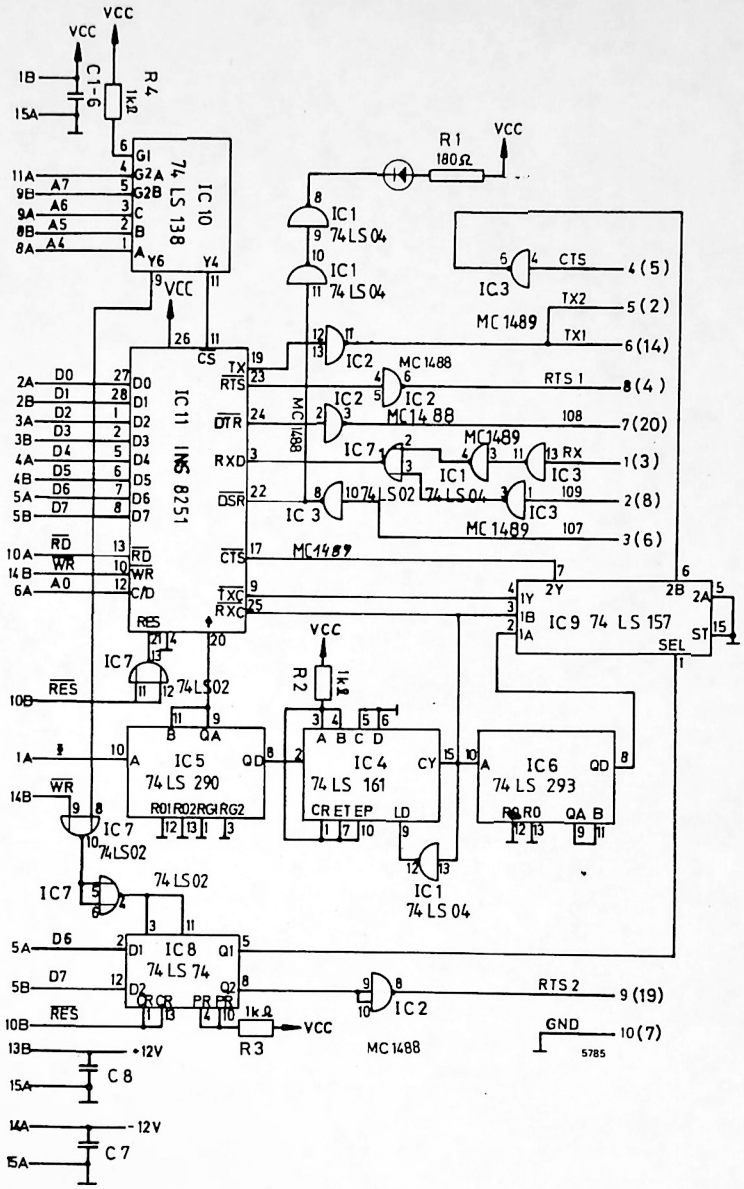


Figure 4.20 LOGIC DIAGRAM VIEWDATA INTERFACE

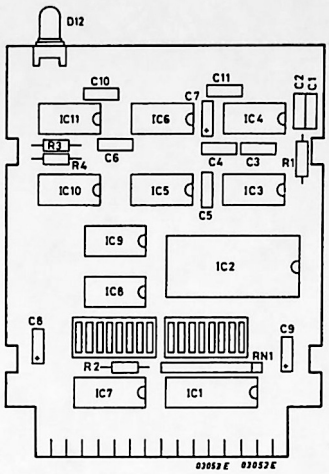


Figure 4.21 COMPONENT LAYOUT SERIAL INTERFACE

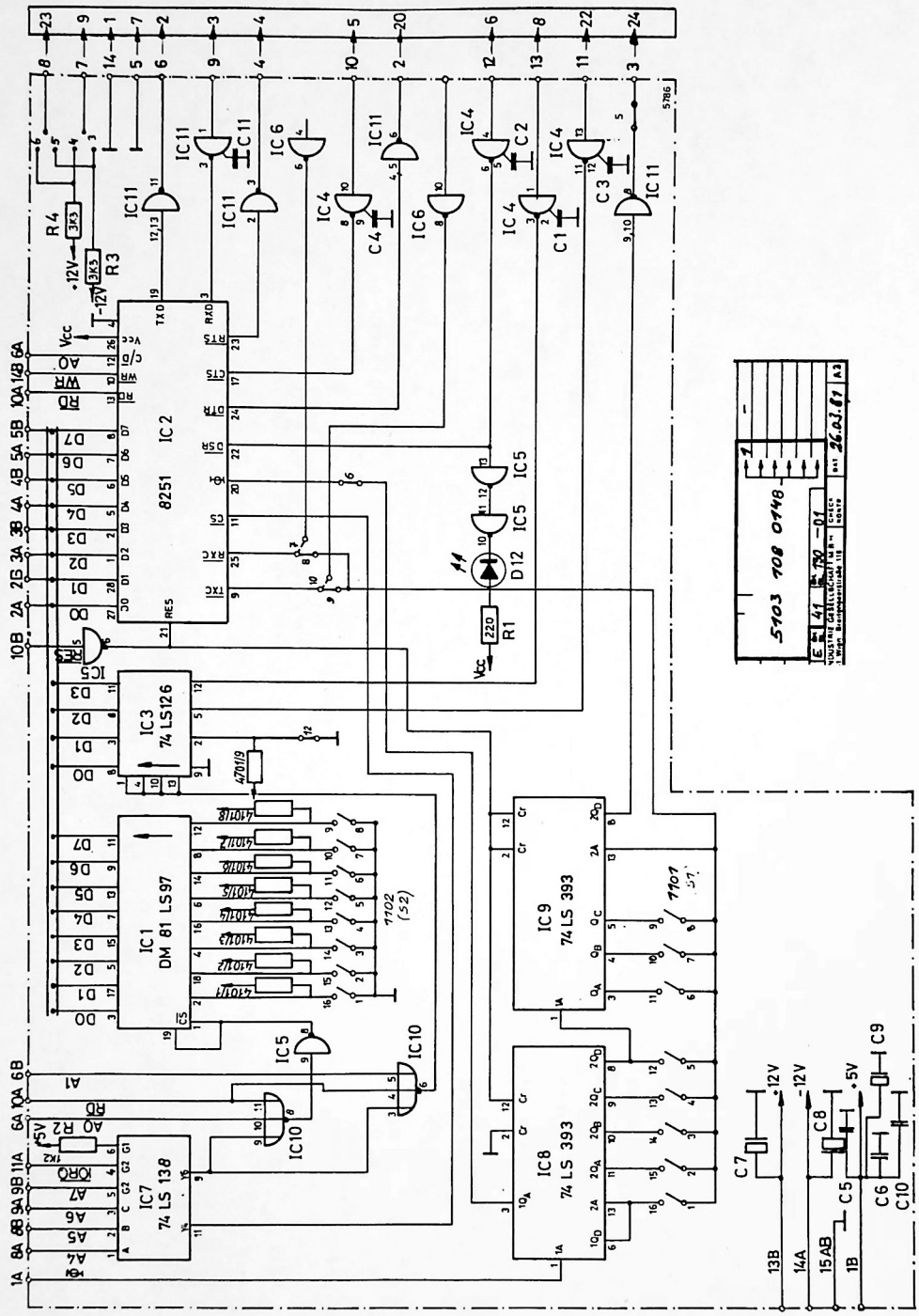
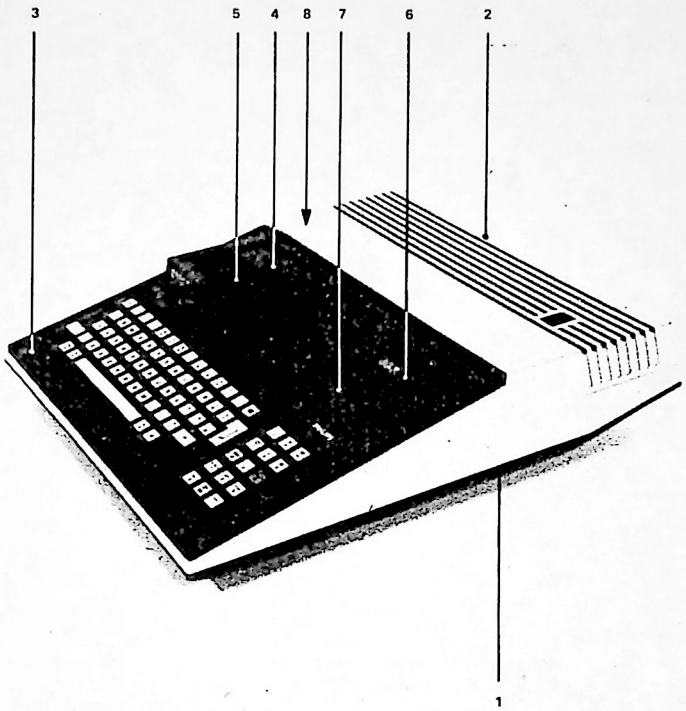


Figure 4.22 LOGIC DIAGRAM SERIAL INTERFACE


3
5
4
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7
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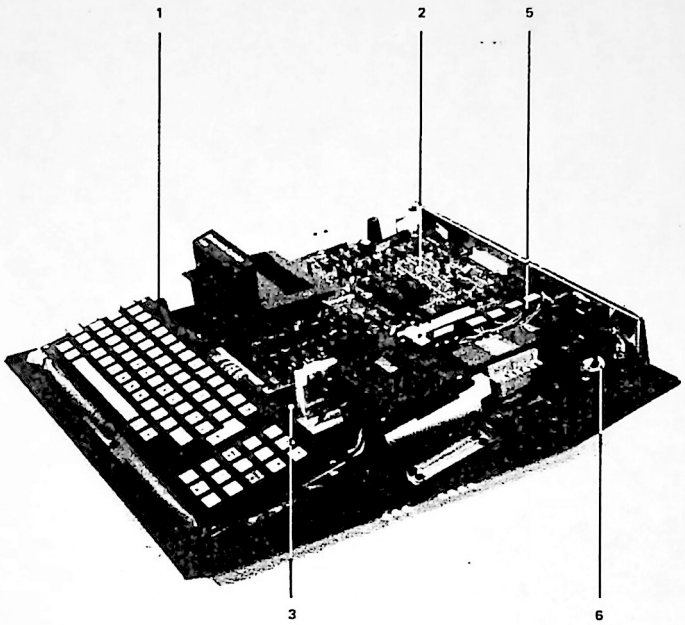
2
1

Pos.	Code Number	Description
A	5103 100 5010	Cabinet compl.
1B	5103 107 52940	Lower cover
2B	5103 107 52950	Upper cover
3B	5103 107 52960	Cover lacquered + printed
4B	5103 104 12240	Push
5B	5103 107 53050	Shaft printed
6B	5103 108 50490	Tape deck MDCR 220
7B	5103 104 12330	Transparent cover (not on the picture)
8B	5103 101 40770	Bracket (at the underside of the upper cover)


1
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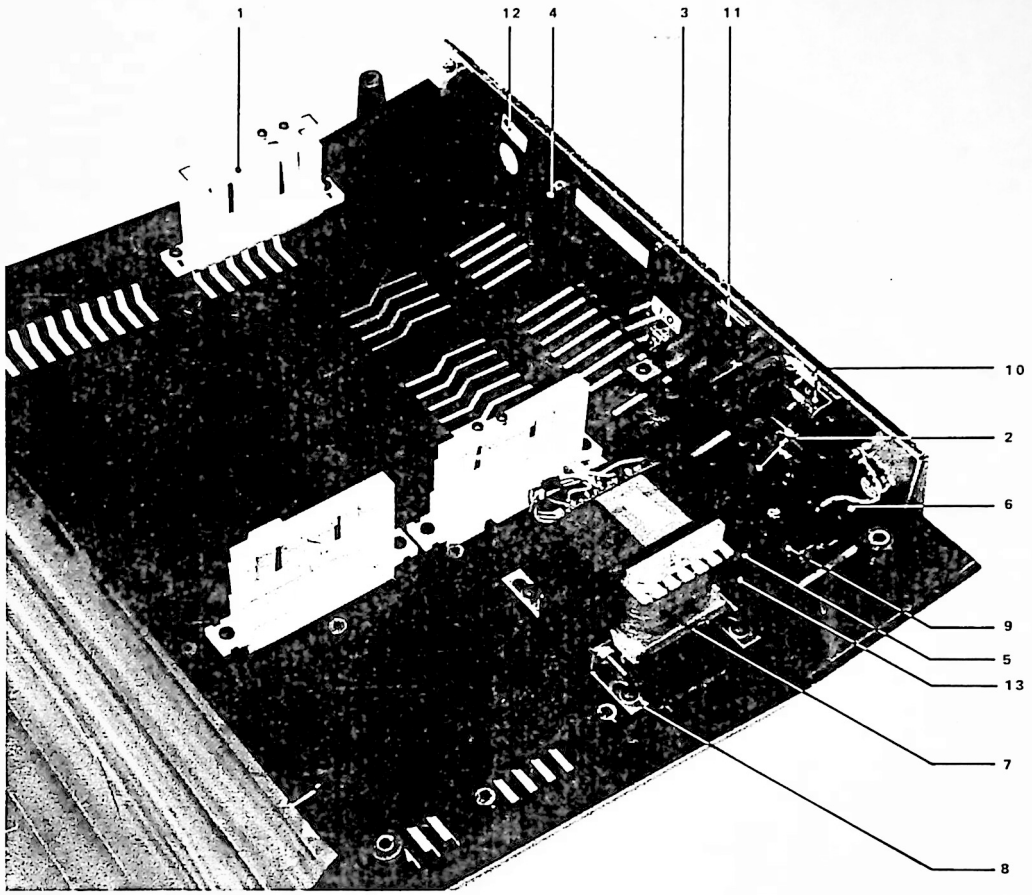
3
6

CABINET BUSINESS VERSION

Pos.	Code Number	Description
1B	5103 108 00480	PCB Keyboard
2B	5103 108 00520	PCB Extension Board
3B	5103 108 01220	PCB Video Board
4B	5103 108 00500	PCB CPU (Business) Board (below video board)
5B	5103 108 00470	PCB PSU
6B	4322 020 97070	Ferritring

CABINET ECONOMY VERSION

Pos.	Code Number	Description
1B	5103 108 00480	PCB Keyboard
2B	5103 108 00520	PCB Extension Board
3B	5103 108 01210	PCB CPU (Economy) Board
5B	5103 108 00470	PCB PSU
6B	4322 020 97070	Ferritring


1
12
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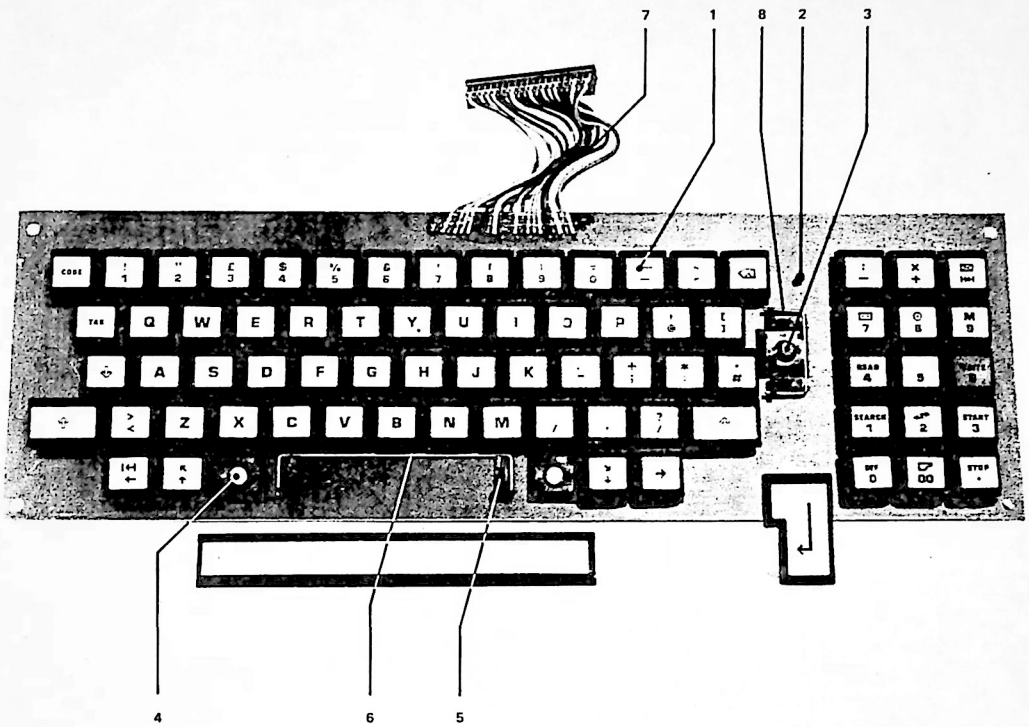
8

Pos.	Code Number	Description
1B	5103 104 12130	Leading
2B	5103 104 12120	Knob
3B	5103 107 53320	Back plate printed
4B	5103 104 12140	Leading
5B	3103 209 11670	Mains switch
6B	5722 660 20880	Mains connector
7B	3112 318 37190	Mains transformer
8B	5103 101 40880	Bracket
9B	5103 101 40760	Plate
10B	5103 101 40780	Strip
11B	5103 101 40800	Bracket
12B	5103 101 40900	Plate
13B	3103 264 02020	Mask


7
1
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2
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4
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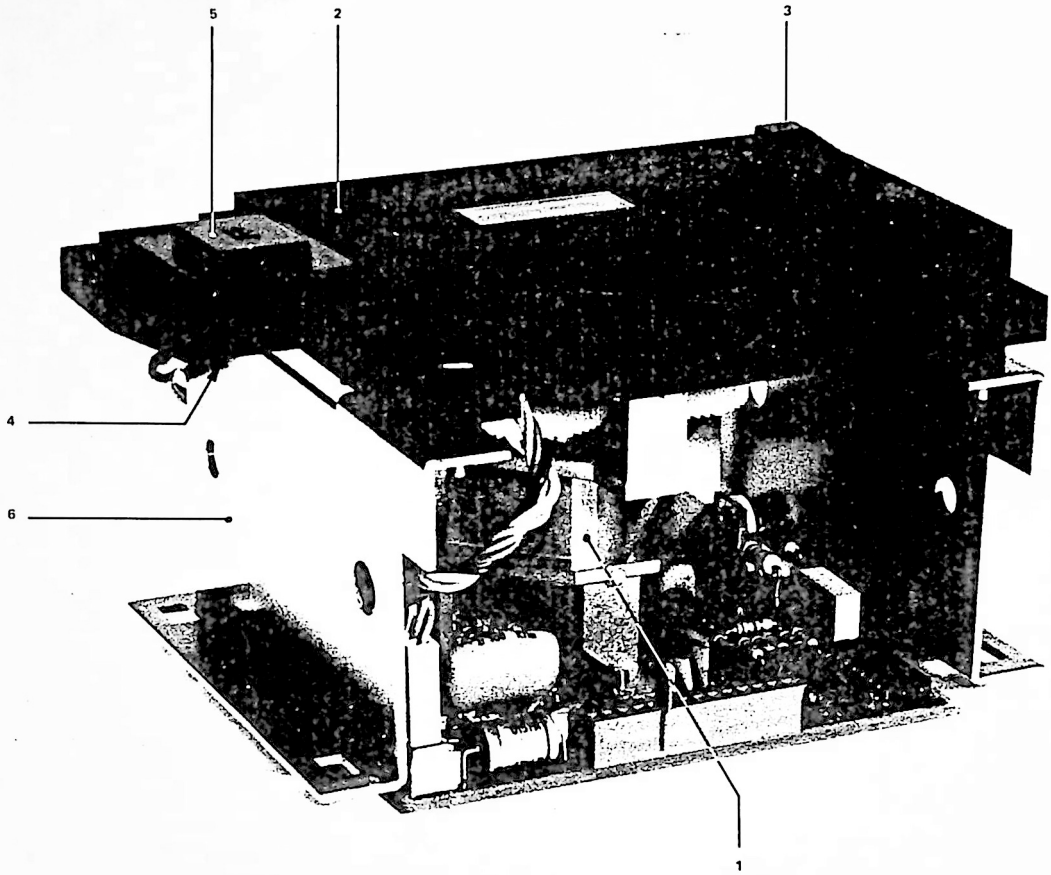
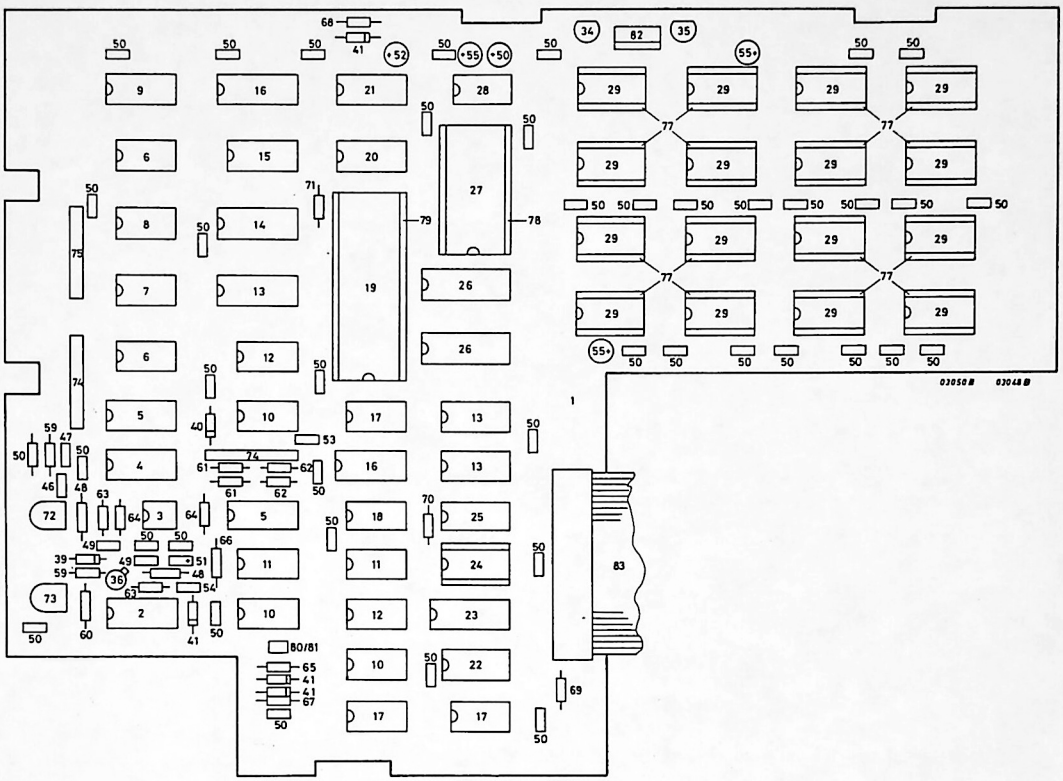
5

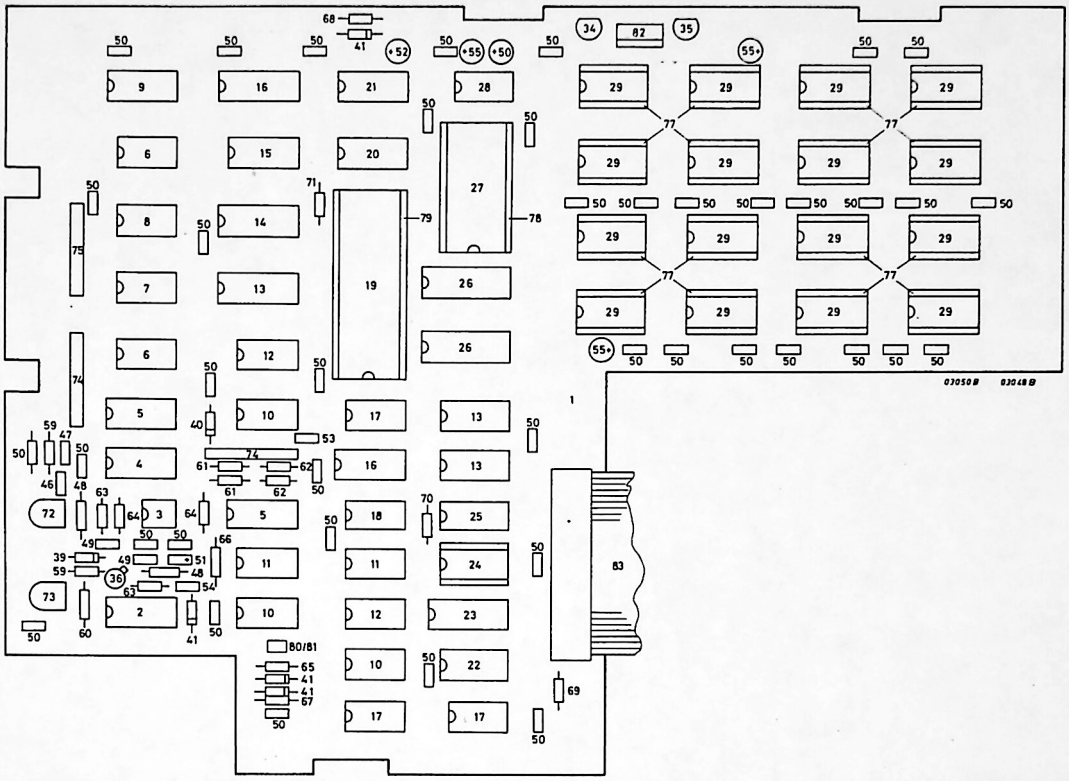
Pos.	Code Number	Description
B	5103 108 00480	Keyboard compl.
1C	5103 108 50410	Keytop for Germany
	5103 108 50450	Keytop for United Kingdom
	5103 108 50530	Keytop for the Netherlands
	5103 108 50440	keytop for Sweden
	5103 108 51240	Keytop for Spain
	5103 107 53860	Keytop for France
2C	9333 203 30112	LED
3C	5112 291 43290	Switch
4C	5112 291 42910	Switch
5C	5122 211 51180	Guiding
6C	5103 101 00750	Bracket
7C	5103 107 80460	Cable
8C		Bracket


5
2
3
4
6
1

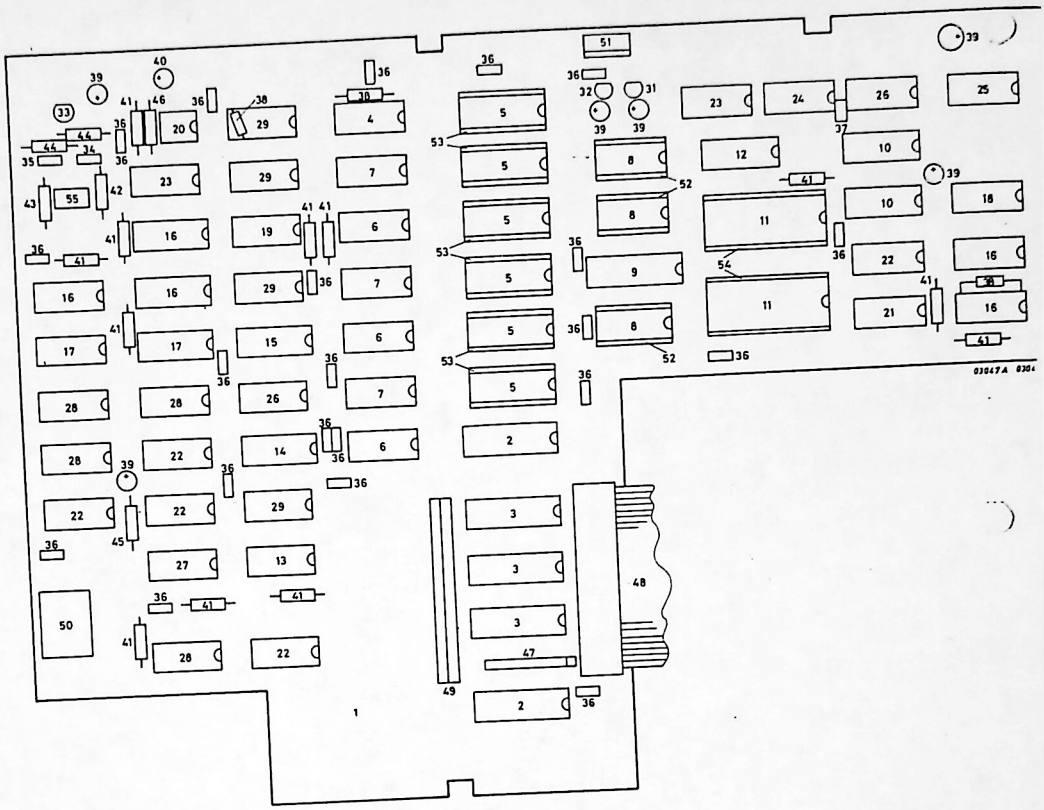
Pos.	Code Number	Description
B	5103 108 50490	Tape deck compl.
1C	3933 536 08230	MDCR 220 tape deck
2C	5103 107 53080	Cover plate assy.
3C	5103 104 12360	Knob
4C	3122 118 43190	Key switch assy.
5C	5103 104 12340	Knob
6C	5103 101 40790	Bracket



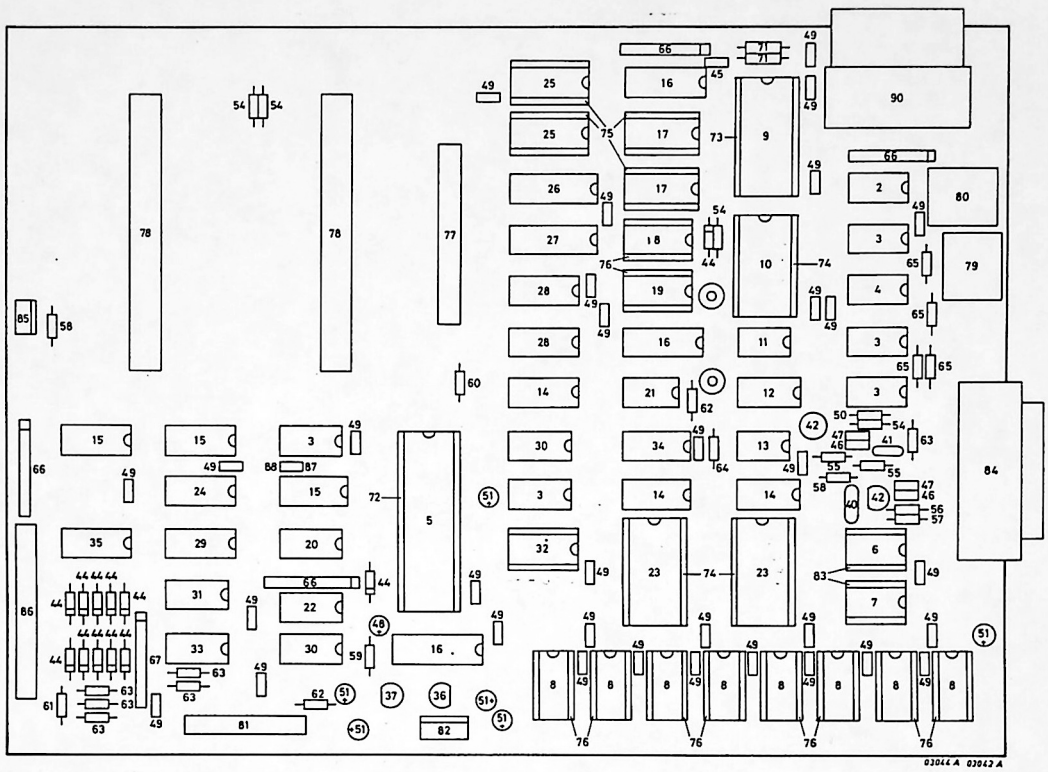
Pos.	Code Number	Description
1B	5103 108 00523	PCB Extension board compl.
2B	9332 201 50682	IC MC4024P
3B	9332 404 20112	IC µA741CN
4B	9335 949 80682	IC AM26502PC
5B	9332 877 80112	IC N74S112N
6B	9332 830 60112	IC 705MIN7406A
7B	9332 871 10112	IC N74LS38A
8B	9332 864 20112	IC N7414A
9B	9332 873 90112	IC 74LS153N
10B	9334 617 20112	IC N74LS74AN
11B	9332 886 70112	IC N74LS02A
12B	9332 869 00112	IC N74LS00A
13B	9332 874 00112	IC N74LS157B
14B	9332 873 60112	IC N74LS139N
15B	9332 869 30112	IC N74LS04A
16B	9332 874 90112	IC N74LS175N
17B	9332 870 90112	IC N74LS32A
18B	9332 870 70112	IC N74LS27A
19B	9335 284 70682	IC PD 765
20B	9334 510 30112	IC N74SL161AN
21B	9332 873 30112	IC N74LS123B
22B	9332 873 50112	IC N74LS138B
23B	9334 452 40112	IC DM81LS97
24B	5103 108 01140	IC 123N
25B	9335 043 40112	IC N74LS367N
26B	9334 908 00682	IC DP 8304
27C	3103 200 57300	IC Z80
28C	9333 700 70112	IC N74LS125
29C	9334 247 50112	IC RAM MK 4116-4
34C	9335 183 30682	IC Voltage reg. LM79 L12 Neg.
35C	9335 183 20682	IC Voltage reg. LM79 L05 Neg.
36C	9330 894 90112	Transistor 2N2222A
39C	9331 177 40113	Diode BZX79/C6V2
40C	9331 177 30113	Diode BZX79/C5V6
41C	9330 839 90112	Diode 1N4148
46C	2222 631 05221	Capacitor 220pF 100V
47C	2222 631 04479	Capacitor 47pF 100V
48C	2222 424 21302	Capacitor 1,3nF 63V
49C	8203 235 09260	Capacitor 47nF 63V
50C	2012 572 10011	Capacitor 100nF 63V
51C	2013 017 01005	Capacitor 0,47µF 35V
52C	2013 017 01157	Capacitor 47µF 10V
53C	2222 629 03102	Capacitor 1nF 63V
54C	2222 031 28101	Capacitor 100pF 63V
55C	2013 017 01030	Capacitor 33µF 16V
59C	2322 211 23512	Resistor 5K1
60C	2322 211 23271	Resistor 270E
61C	2322 211 23222	Resistor 2K2
62C	2322 151 23482	Resistor 3K48



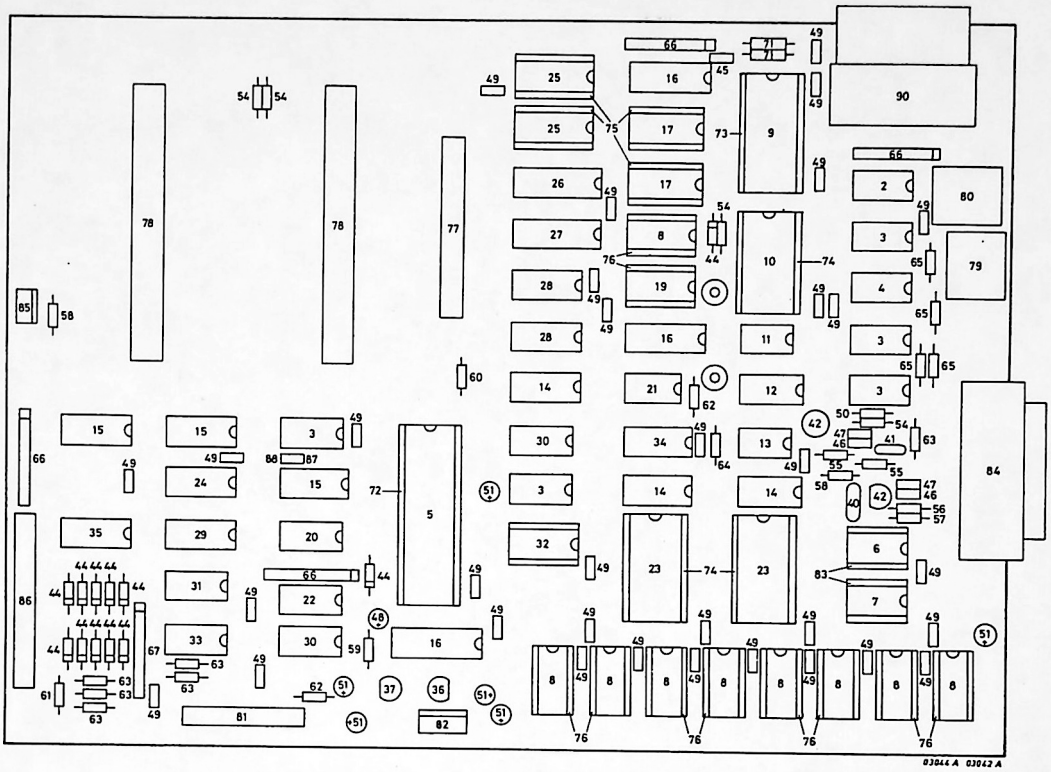
Pos.	Code Number	Description
64C	2322 151 21003	Resistor 10K
65C	2322 211 23122	Resistor 1K2
66C	2322 212 23161	Resistor 160E
67C	2322 211 23102	Resistor 1K0
68C	2322 211 23104	Resistor 100K
69C	2322 211 23331	Resistor 330E
70C	2322 211 23472	Resistor 4K7
71C	2322 211 23391	Resistor 390E
72C	2322 482 20223	Resistor 22K
73C	2322 482 20332	Resistor 3K3
74C	3103 200 57748	Resistor Network
75C	2122 118 00193	Resistor Network
77C	5103 108 70200	IC Socket 16 pins
78C	3103 238 73260	IC Socket 28 pins
79C	3103 238 73270	IC Socket 40 pins
80C	3103 238 74050	Stik-headers
81C	3103 238 74040	Connector
82C	2422 025 02522	Cable 5P
83C	5013 107 80410	Cable 40P



Pos.	Code Number	Description
1B	5103 108 01220	PCB Video board compl.
2C	9334 908 00112	IC DP 8304
3C	9334 452 40112	IC D.M. 81LS97
4C	9334 452 00112	IC INT3216
5C	9334 294 50112	IC HM472114/4
6C	9332 874 00112	IC N74LS157B
7C	9334 510 30112	IC N74LS161AN
8C	9334 682 90112	IC MK1007P
9C	9334 121 80112	IC 74LS273
10C	9332 874 90112	IC SN74LS175B
11C	9335 702 80112	IC MASK. ROM. 4K x 8
12C	3103 200 57320	IC SN74LS166
13C	9332 972 60112	IC N74LS85B
14C	9332 873 60112	IC N74LS139N
15C	9332 874 00112	IC N74LS157B
16C	9334 510 40112	IC N74LS163B
17C	9332 873 50112	IC N74LS138B
18C	9332 872 90112	IC N74LS109B
19C	9332 865 80112	IC N74107A
20C	9332 243 90112	IC NE555V
21C	9332 869 70112	IC N74LS10A
22C	9332 886 70112	IC N74LS02A
23C	9332 869 80112	IC N74LS11
24C	9332 872 20112	IC N74LS86A
25C	9332 869 50112	IC N74LS08A
26C	9332 870 90112	IC N74LS32A
27C	9332 414 00112	IC N74LS00A
28C	9332 870 70112	IC N7439N
29C	9332 869 00112	IC N74LS00A
31C	9335 183 20112	Voltage reg. IC LM79 L06 Neg.
32C	9335 183 30112	Voltage reg. IC LM79 L12 Neg.
33C	9331 977 30112	Transistor BC558
34C	2222 642 10229	Capacitor 22pF 100V
35C	2222 642 10689	Capacitor 69pF 100V
36C	2012 572 10011	Capacitor 100nF 63V
37C	2222 630 03471	Capacitor 470pF 100V
38C	2011 554 16002	Capacitor 1nF 160V
39C	2013 017 01031	Capacitor 33µF 16V
40C	2013 017 01007	Capacitor 1µF 35V
41C	2322 211 23102	Resistor 1K
42C	2322 211 23183	Resistor 18K
43C	2322 211 23273	Resistor 27K
44C	2322 211 23361	Resistor 360E
45C	2322 211 23121	Resistor 120E
46C	2322 211 23684	Resistor 680K
47C	3103 200 57740	Resistor Network
48C	5103 103 80410	Cable
49C	2422 025 01899	Connector 20 poles
50C	2422 026 00417	Connector Hirschmann 5 poles
51C	2422 025 02522	Connector 5 poles


03044 A 03042 A

Pos.	Code Number	Description
1B	5103 108 01210	PCB Economy CPU compl.
2C	9332 872 20112	IC N74LS86A
3C	9334 617 20112	IC N74LS74AN
4C	9332 886 70112	IC N74LS02A
5C	3103 200 57620	IC Z80-CPU ZILOG MOSTEK
6C	9332 912 00112	IC MC1489
7C	9332 963 20112	IC MC1488
8C	9334 247 50112	IC RAM MK4116-4
9C	9335 036 70112	IC SAA5051
10C	9334 286 70112	IC SAA5020
11C	9332 869 00112	IC N74LS00A
12C	9332 826 10112	IC HEF4022BP
13C	9332 876 60112	IC N74LS293A
14C	9332 874 00112	IC N74LS157B
15C	9332 825 80112	IC HEF40097BP
16C	9334 452 40112	IC DM81LS97
17C	9334 294 50682	IC RAM HM472114/4
18C	5103 108 01120	IC 825 129N
19C	5103 108 01130	IC 825 129N
20C	9332 873 40112	IC SN74LS132
21C	9332 869 30112	IC N74LS04A
22C	9332 869 90112	IC N74LS12A
23C	9335 702 60112	IC MASK ROM 4K x 8
24C	9332 874 80112	IC N74LS174B
25C	8203 235 09230	IC INTEL RAM 2114A-4
26C	9334 908 00682	IC DP8304
27C	9334 121 80112	IC 74LS273
28C	9332 875 40112	IC N74LS193B
29C	9332 873 50112	IC N74LS138B
30C	9332 870 90112	IC N74LS32A
31C	9332 014 50112	IC SN7416
32C	5013 108 01110	IC 82S123N
33C	9332 776 10112	IC HEF4013BP
34C	9334 510 30112	IC N74LS161AN
35C	9332 873 70122	IC N74LS145B
36C	9335 183 30682	Voltage regulator LM79 L12 Neg.
37C	9335 183 20682	Voltage regulator LM79 L05 Neg.
40C	8203 235 08310	Quartz 20MHz RW43
41C	8203 235 08290	Quartz 6MHz RW43
42C	9331 977 30112	Transistor BC558
44C	9330 839 90711	Diode 1N148
45C	2222 630 03471	Capacitor 470pF 100V
46C	2222 642 10229	Capacitor 22pF 100V
47C	2222 642 10689	Capacitor 68pF 100V
48C	2013 017 01012	Capacitor 4,7µF 35V
49C	2012 572 10011	Capacitor 100nF 63V
50C	2013 017 01107	Capacitor 15µF 35B
51C	2013 017 01031	Capacitor 33µF 16V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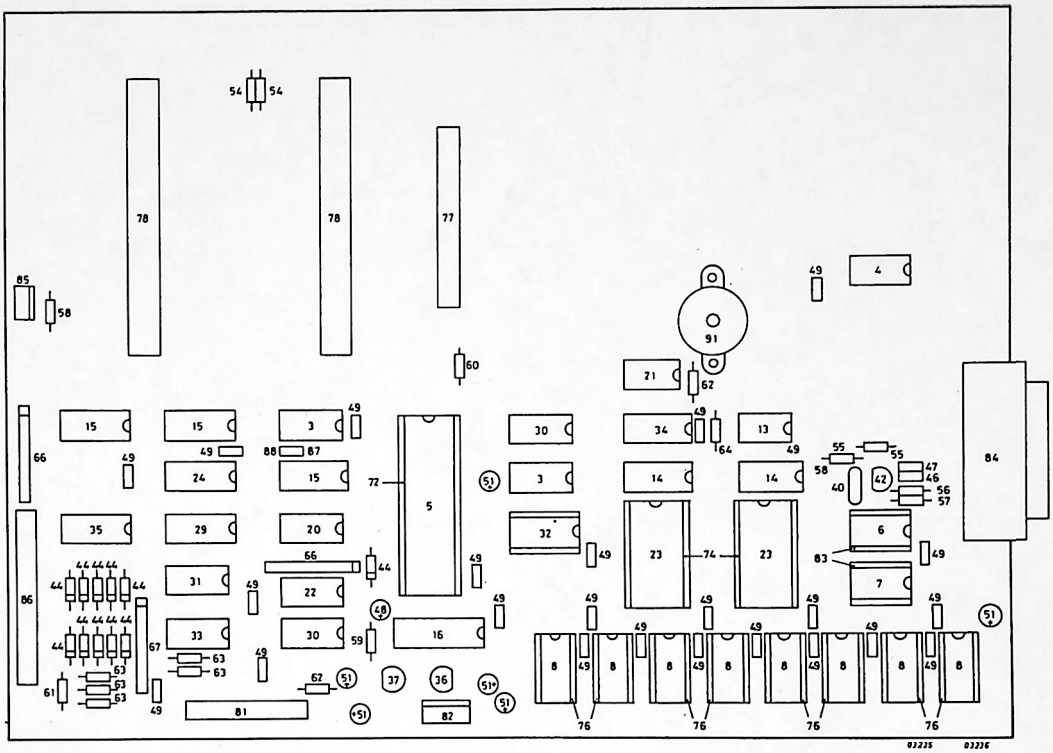
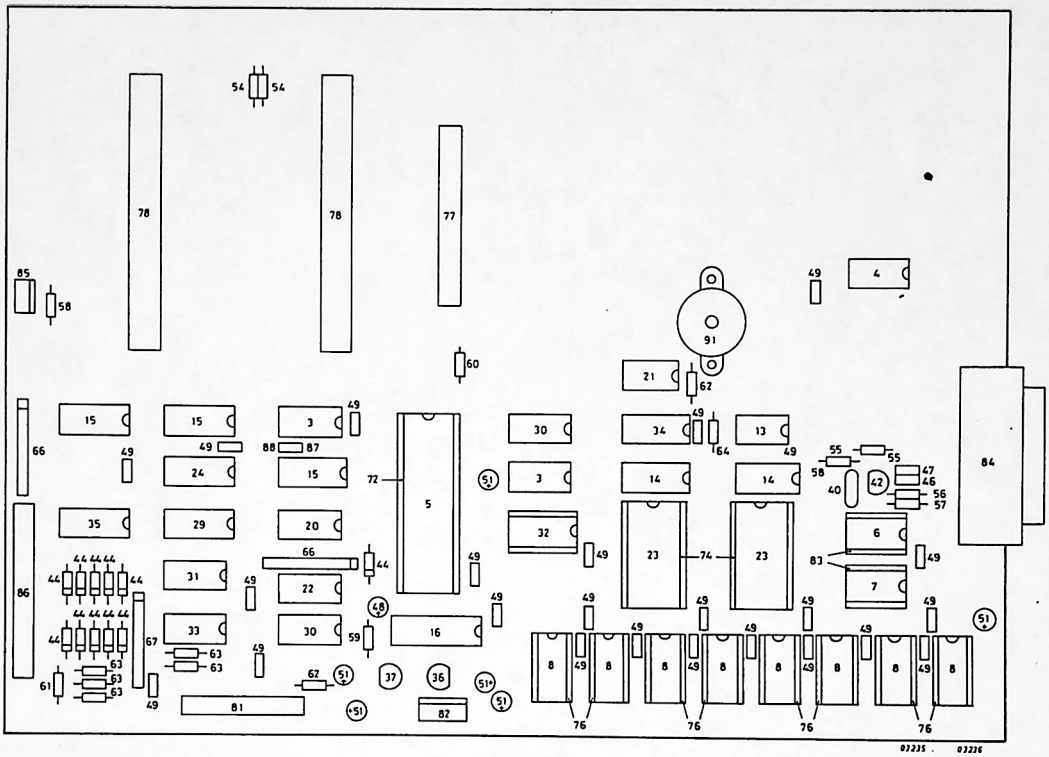
Pos.	Code Number	Description
54C	2322 211 23102	Resistor 1K
55C	2322 211 23273	Resistor 27K
56C	2322 211 23183	Resistor 18K
57C	2322 211 23391	Resistor 390E
58C	2322 211 23181	Resistor 180E
59C	2322 211 23393	Resistor 39K
60C	2322 211 23331	Resistor 330E
61C	2322 211 23271	Resistor 270E
62C	2322 211 23472	Resistor 4K7
63C	2322 211 23124	Resistor 120K
64C	2322 211 23471	Resistor 470E
65C	2322 211 23121	Resistor 120E
66C	3103 200 57740	Resistor network 4310R-101-472
67C	2122 118 00199	Resistor network 4308R-101-683
71C	2413 535 00322	Coil 100µH
72C	3103 238 73270	IC Socket 40 pins
73C	3103 238 73260	IC Socket 28 pins
74C	3103 238 73250	IC Socket 24 pins
75C	5103 108 70220	IC Socket 18 pins
76C	5103 108 70200	IC Socket 16 pins
77C	2422 025 01899	Connector 20 poles
78C	2422 025 03584	Connector Molex 6511
79C	2422 026 01225	Socket 6 pins MAB 6H
80C	2422 031 10179	Bush
81C	2422 025 03355	Connector 14 poles
82C	2422 025 03345	Connector 5 poles
83C	3103 238 73430	IC Socket 14 pins
84C	5103 108 70660	Connector V-24
85C	2422 025 03343	Connector 3 pins
86C	2422 025 03362	Connector 20 pins
87C	3103 238 74050	Stik-header 2 pins
88C	3103 238 74040	Connector 2 pins

NOT INCLUDED

90C	5103 108 51060	Modulator UHF
90C	5103 108 72150	Modulator VHF
X D	5103 108 01380	PCB Modulator UHF compl.
D	5103 108 00540	PCB Modulator VHF compl. 2.6 2.65,
D	5103 107 52710	Can treatment
D	3122 131 20060	Cover
D	3122 137 51210	Block



Pos.	Code Number	Description
1B	5103 108 00500	PCB Business CPU compl.
3C	9334 617 20112	IC N74LS74AN
4C	9332 886 70112	IC N74LS02A
5C	3103 200 57620	IC Z80-CPU ZILOG MOSTEK
6C	9332 912 00112	IC MC1489
7C	9332 963 20112	IC MC1488
8C	9334 247 50112	IC RAM MK4116-4
13C	9332 876 60112	IC N74LS293A
14C	9332 874 00112	IC N74LS157B
15C	9332 825 80112	IC HEF40097BP
16C	9334 452 40112	IC DM81LS97
20C	9332 873 40112	IC SN74LS132
21C	9332 869 30112	IC N74LS04A
22C	9332 869 90112	IC N74LS12A
23C	9335 702 60112	IC MASK ROM 4K x 8
24C	9332 874 80112	IC N74LS174B
29C	9332 873 50112	IC N74LS138B
30C	9332 870 90112	IC N74LS32A
31C	9332 014 50112	IC SN7416
X 32C	5013 108 01110	IC 82S123N
33C	9332 776 10112	IC HEF4013BP
34C	9334 510 30112	IC N74LS161AN
35C	9332 873 70122	IC N74LS145B
36C	9335 183 30682	Voltage regulator LM79 L12 Neg.
37C	9335 183 20682	Voltage regulator LM79 L05 Neg.
40C	8203 235 08310	Quartz 20MHz RW43
42C	9331 977 30112	Transistor BC558
44C	9330 839 90711	Diode 1N1148
46C	2222 642 10229	Capacitor 22pF 100V
47C	2222 642 10689	Capacitor 68pF 100V
48C	2013 017 01012	Capacitor 4,7µF 35V
49C	2012 572 10011	Capacitor 100nF 63V
50C	2013 017 01107	Capacitor 15µF 35V
51C	2013 017 01031	Capacitor 33µF 16V
54C	2322 211 23102	Resistor 1K
55C	2322 211 23272	Resistor 27K
56C	2322 211 23183	Resistor 18K
57C	2322 211 23391	Resistor 390E
58C	2322 211 23181	Resistor 180E
59C	2322 211 23393	Resistor 39K
60C	2322 211 23331	Resistor 330E
61C	2322 211 23271	Resistor 270E
62C	2322 211 23472	Resistor 4K7
63C	2322 211 23124	Resistor 120K
64C	2322 211 23471	Resistor 470E
66C	3103 200 57740	Resistor network 4310R-101-472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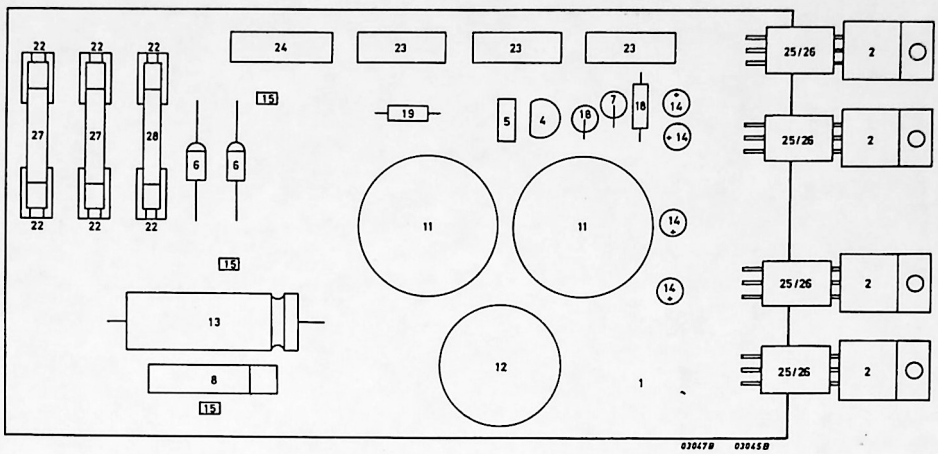
Pos.	Code Number	Description
67C	2122 118 00199	Resistor network 4308R-101-683
72C	3103 238 73270	IC Socket 40 pins
74C	3103 238 73250	IC Socket 24 pins
76C	5103 108 70200	IC Socket 16 pins
77C	2422 025 01899	Connector 20 poles
78C	2422 025 03584	Connector Molex 6511
81C	2422 025 03355	Connector 14 poles
82C	2422 025 03345	Connector 5 poles
83C	3103 238 73430	IC Socket 14 pins
84C	5103 108 70660	Connector V-24
85C	2422 025 03343	Connector 3 pins
86C	2422 025 03362	Connector 20 pins
87C	3103 238 74050	Stik-header 2 pins
88C	3103 238 74040	Connector 2 pins
91C	5103 108 70670	KER. Resonator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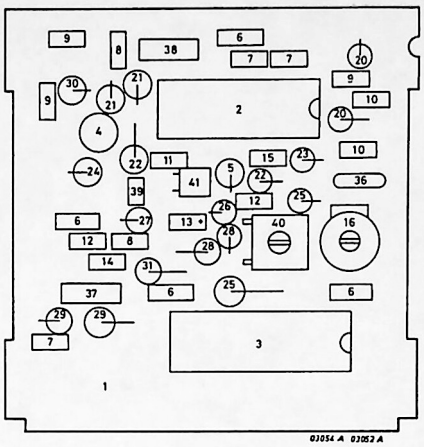
03045B

Pos.	Code Number	Description
1B	5103 108 00470	PCB PSU compl.
2C	9332 996 00112	Voltage regulator
3C	9332 996 60112	Voltage regulator
4C	9331 976 40112	Transistor BCS48
5C	9332 642 80112	Transistor BD675
6C	9332 116 80112	Diode 1N5401
7C	9331 176 90112	Diode BZX79 C3V9
8C	9330 873 30112	Rectifier BY164
11C	2222 033 45682	Capacitor 6800µF 16V
12C	2222 033 46332	Capacitor 3300µF 25V
13C	2222 032 16471	Capacitor 470µF 25V
14C	2013 017 0105	Capacitor 10µF 35V
15C	2222 629 01103	Capacitor 10nF 63V
18C	2322 211 23472	Resistor 4K7
19C	2322 211 23102	Resistor 1K
22C	5103 101 00020	Fuse holder
23C	2422 025 02522	Connector 5 poles
24C	2422 025 02523	Connector 6 poles
25C	3103 308 70690	Socket
26C	3103 221 05370	Contact spring
27C	2422 086 00033	Fuse 1A
28C	2422 086 00049	Fuse 5A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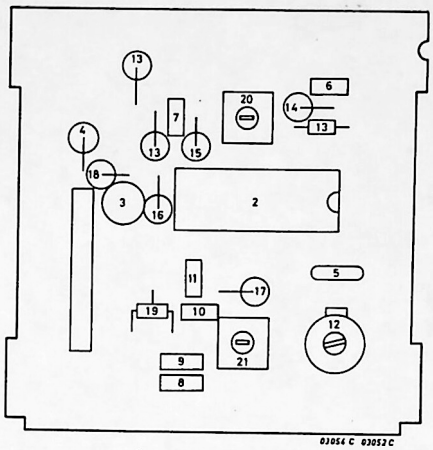
03054 A 03052 A

Pos.	Code Number	Description
C	5103 108 72150	Modulator VHF
1D	5103 108 00540	PCB Modulator board VHF compl.
2E	9335 203 50682	IC LM1889
3E	9335 203 40682	IC LM1886
4E	9331 492 00112	Transistor BC337
5E	9333 201 80113	Diode CF420
6E	2012 572 10011	Capacitor 100nF 63V
7E	2222 631 10101	Capacitor 100pF 100V
8E	2222 631 10689	Capacitor 68pF 100V
9E	2222 629 01103	Capacitor 10nF 63V
10E	2222 631 10399	Capacitor 39pF 100V
11E	2222 631 10479	Capacitor 47pF 100V
12E	2222 631 10339	Capacitor 33pF 100V
13E	8203 235 09000	Capacitor 3,3µF 16V
14E	2222 631 10279	Capacitor 27pF 100V
15E	2222 631 10229	Capacitor 22pF 100V
16E	2222 808 11279	Trim capacitor 2/30pF
20E	2322 211 23102	Resistor 1K
21E	2322 211 23221	Resistor 220E
22E	2322 211 23133	Resistor 15K
23E	2322 211 23562	Resistor 5K6
24E	2322 211 23561	Resistor 560E
25E	2322 211 23332	Resistor 3K3
26E	2322 211 23473	Resistor 47K
27E	2322 211 23121	Resistor 120E
28E	2322 211 23563	Resistor 56K
29E	2322 211 23689	Resistor 68E
30E	2322 211 23181	Resistor 180E
31E	2322 211 23222	Resistor 2K2
32E	2322 210 23331	Resistor 330E
33E	2322 210 23272	Resistor 2K7
36E	4322 143 04040	Quartz 4,433619 MHz
37E	5103 108 20100	Coil
38E	5103 108 20110	Coil
39E	5103 108 20120	Coil
40E	3103 138 23650	Coil
41E	5103 108 20140	Coil
42D	5103 107 52710	Can treatment
43D	3122 131 20060	Cover
44D	3122 137 51210	Block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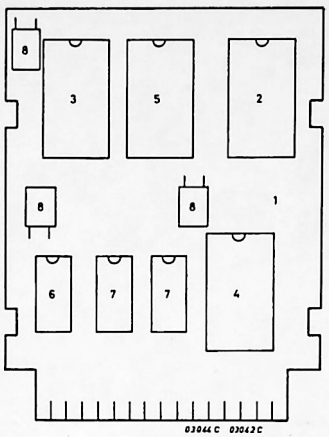
03054 C 03052 C

Pos.	Code Number	Description
C	5103 108 51060	Modulator UHF
1D	5103 108 01380	PCB modulator UHF compl.
2E	9334 997 80112	IC PE 1X
3E	9331 976 80112	Transistor BC549
4E	9331 177 90113	Diode BZX79/C10
5E	4322 143 04050	Quartz 8,86 MHz
6E	2222 631 10189	Capacitor 18pF 100V
7E	2222 631 10121	Capacitor 120pF 100V
8E	2013 017 01015	Capacitor 10µF 35V
9E	2012 572 10011	Capacior 100nF 63V
10E	2222 631 10339	Capacitor 33pF 100V
11E	2222 629 01103	Capacitor 10nF 63V
12E	2222 808 11279	Trim Capacitor 30pF
13E	2322 211 23122	Resistor 1K2
14E	2322 211 23392	Resistor 3K9
15E	2322 211 23102	Resistor 1K
16E	2322 211 23471	Resistor 470E
17E	2322 211 23182	Resistor 1K8
18E	2322 211 23391	Resistor 390E
19E	2322 482 20472	Trim pot 5K
20E	5103 108 20190	Coil
21E	5103 108 20200	Coil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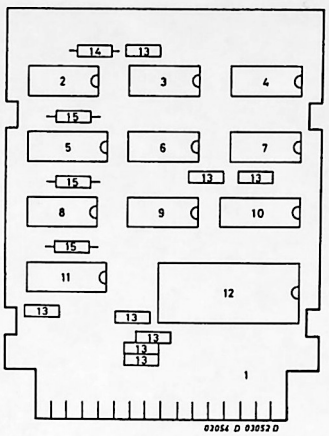
Pos.	Code Number	Description
A		ROM Cartridge
1B	5103 108 00530	PCB ROM cartridge compl.
2C	5103 108 70990	IC ROM 4K x 8
3C	5103 108 72040	IC ROM 4K x 8
4C	5103 108 71010	IC ROM 4K x 8
5C	5103 108 71020	IC ROM 4K x 8
6C	9332 573 50112	IC N74LS138B
7C	9335 043 40112	IC N74LS367N
8C	2012 572 10011	Capacitor 100nF 63V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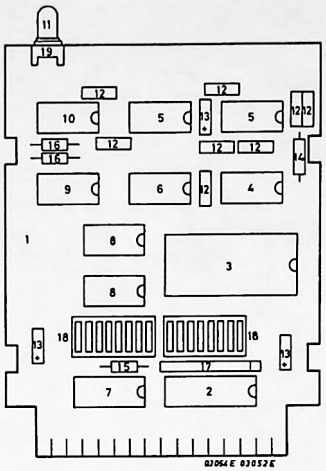
Pos.	Code Number	Description
A		View data interface
1B	5103 108 01240	PCB view data interface compl.
2C	9332 873 50112	IC 74LS138B
3C	9334 282 20112	IC INS 8251
4C	9332 876 50112	IC N74LS290A
5C	9334 510 30112	IC N74LS161AN
6C	9332 876 60112	IC N74LS293A
7C	9332 874 00112	IC N74LS157B
8C	9334 617 20112	IC N74LS74AN
9C	9332 869 30112	IC N74LS04A
10C	9332 963 20112	IC MC1488
11C	9332 912 00112	IC MC1489
12C	9332 886 70112	IC N74LS02A
13C	2012 572 10011	Capacitor 100nF 63V
14C	2322 211 23181	Resistor 180E
15C	2322 211 23102	Resistor 1K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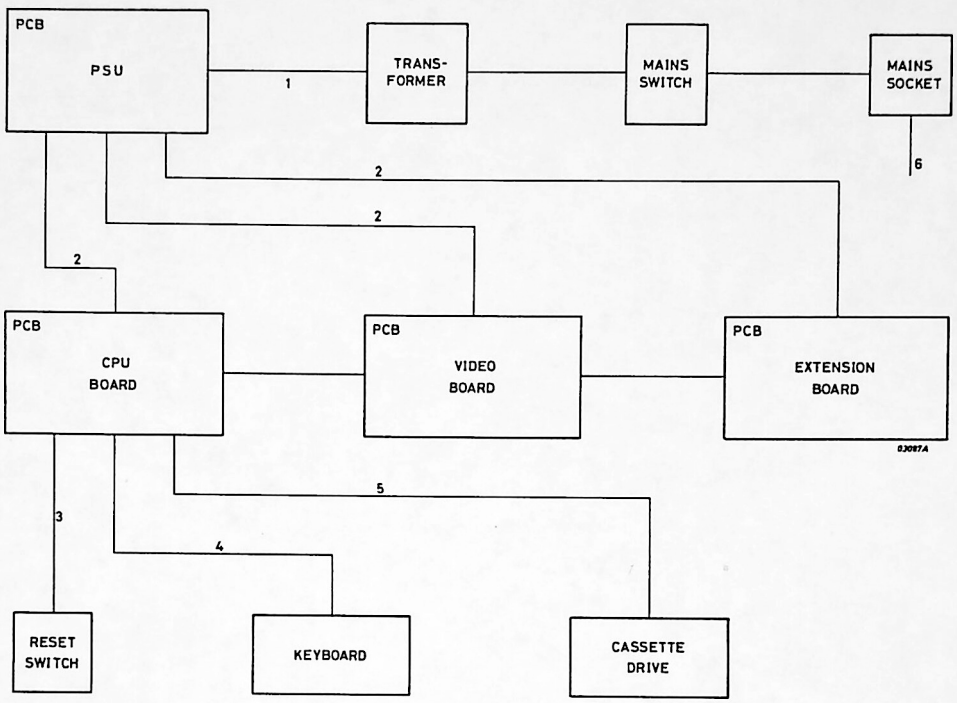
03054E 03052E

Pos.	Code Number	Description
A		Serial Interface
1B	5103 108 01480	PCB Serial Interface compl.
2C	9334 452 40112	IC DM81LS97
3C	9334 282 20682	IC INS8251
4C	9333 700 80112	IC 74LS126N
5C	9332 912 00112	IC MC1489
6C	9332 869 30112	IC N74LS04A
7C	9332 873 50112	IC N74LS138B
8C	9332 278 30112	IC 74LS393
9C	9334 870 70112	IC N74LS27A
10C	9332 963 20112	IC MC1488
11C	9332 184 80112	LED SR103D
12C	2222 640 03103	Capacitor 10nF 63V
13C	2013 017 01005	Capacitor 0,47µF 35V
14C	2322 211 23221	Resistor 220E
15C	2322 211 23122	Resistor 1K2
16C	2322 211 23332	Resistor 3K3
17C	3103 200 57740	Resistor network 4310R-101-472
18C	2422 126 01126	Dip switch
19C	8203 235 10740	LED socket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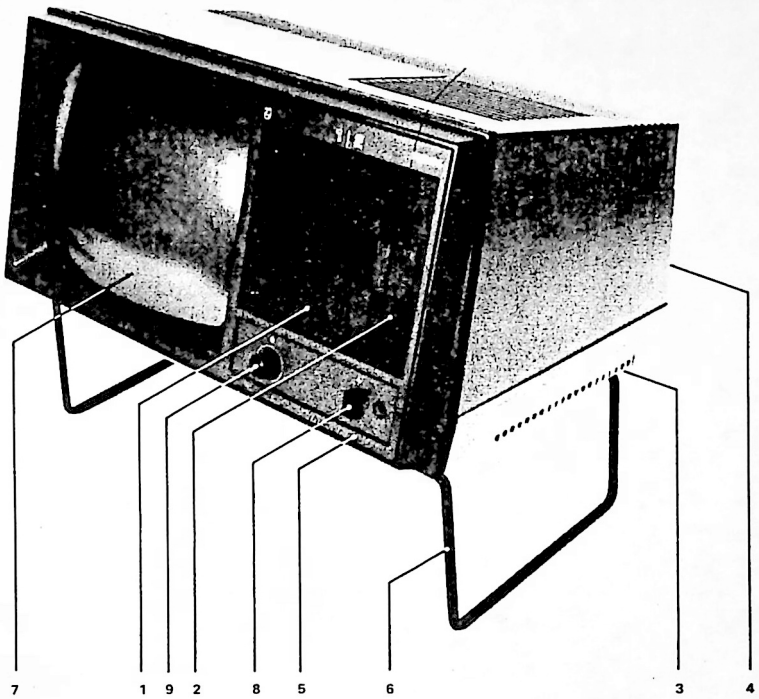
RESET
SWITCH
KEYBOARD
CASSETTE
DRIVE

Pos.	Code Number	Description
1	5103 107 80450	From transformer to PCB PSU
2	5103 107 80470	From PCB PSU to PCB CPU to PCB VIDEO to PCB Extension
3	5103 107 80430	From PCB CPU to reset switch
4	5103 107 80460	From PCB CPU to keyboard
5	5103 107 80440	From PCB CPU to cassette drive
6	5722 660 30670	Mains cable (European)
	5722 660 22320	Mains cable (English)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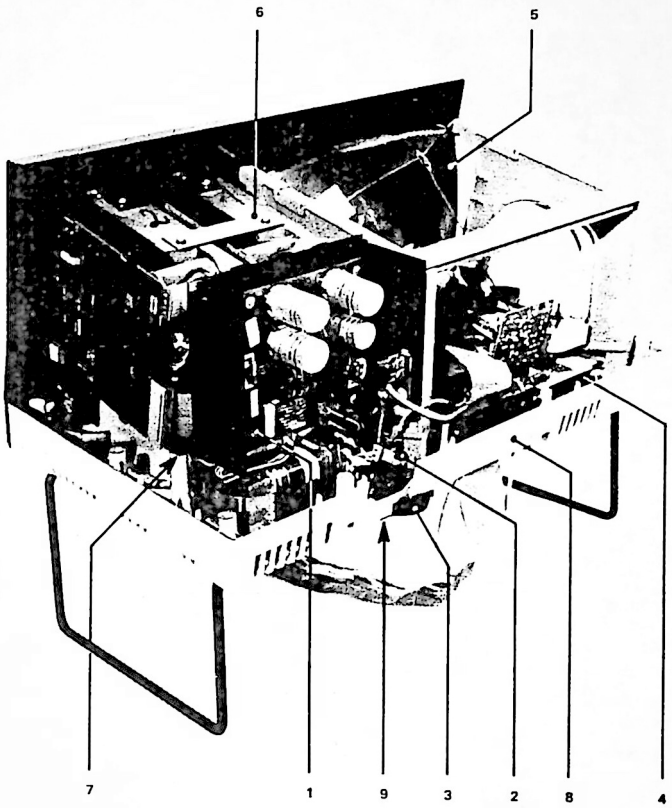
Pos	Code Number	Description
A	5103 108 50360	Monitor compl.
1B	5103 108 50910	Mini Floppy Disc drive
2B	5103 108 50920	Mini Floppy Disc drive
3B	5103 107 52910	Base plate
4B	5103 107 52880	Cover
5B	5103 107 53070	Front Cover
6B	5103 107 52990	Holder
7B	5103 107 53010	Monitor Fimi 90°
8B	5103 104 12120	Knob
9B	5103 104 00230	Turn Knob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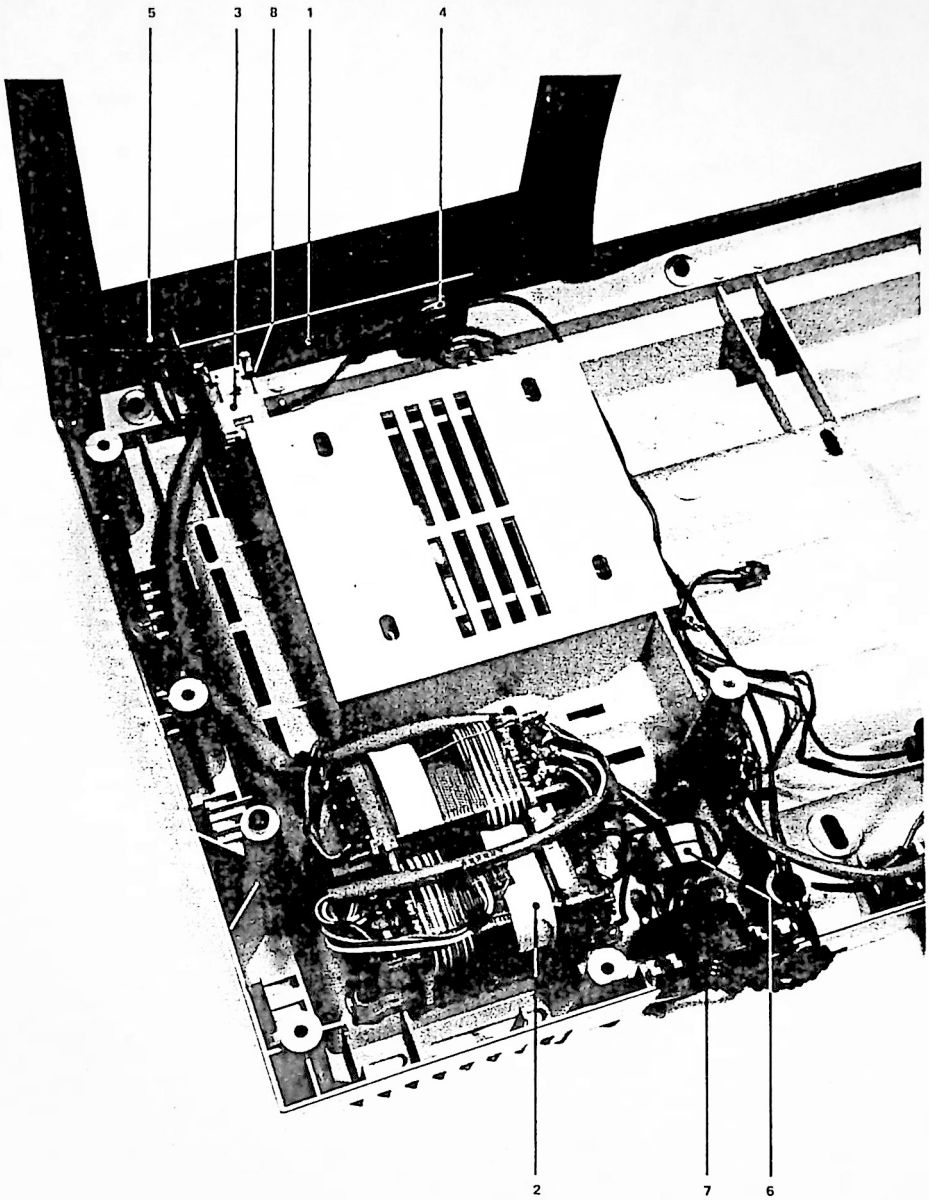
Pos.	Code Number	Description
1B	5103 108 50810	Power supply
2B	5103 100 40210	Screw
3B	5103 104 12210	Knob
B	5103 107 53010	Monitor Fimi 90° + mounting plate
4C	5103 101 40940	Mounting plate
5C	3119 208 89080	Monitor Fimi
6C	5103 101 40750	Link
7C	5103 101 40730	Mounting plate for FDD
8C	5103 107 53310	Plate PVC
9C	5103 101 40740	Plate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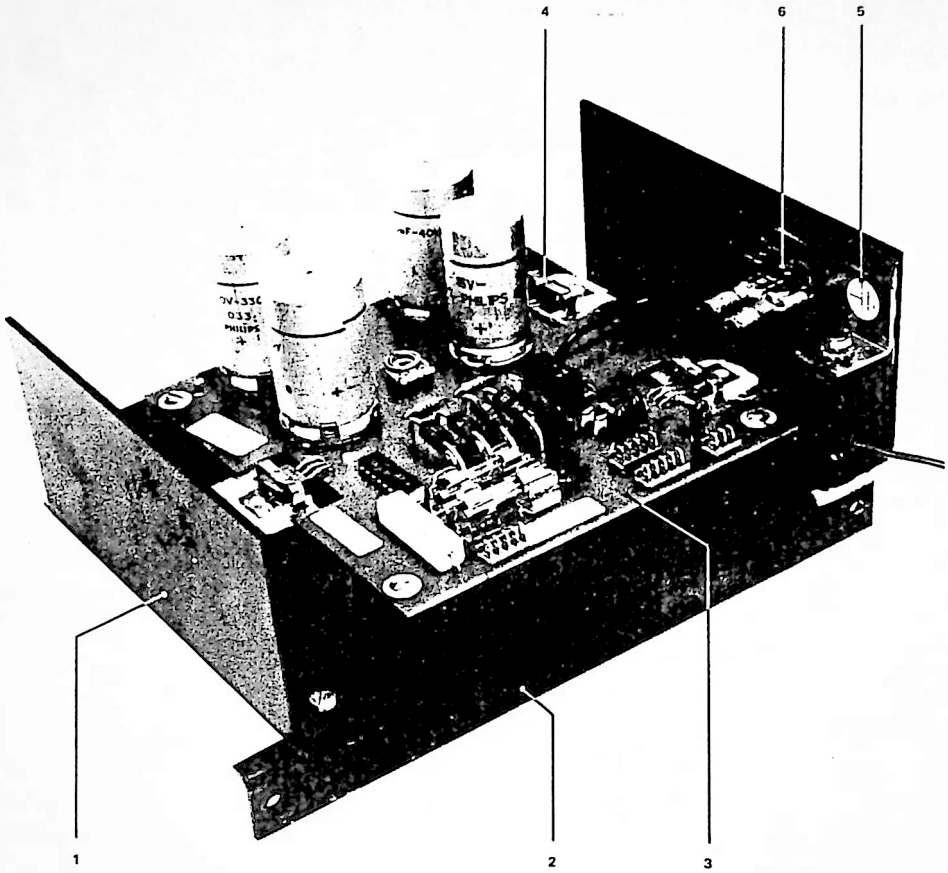
Pos.	Code Number	Description
1B	5103 101 40690	Bracket
2B	3112 318 37280	Mains transformer
3B	3103 209 11670	Mains switch
4B	2322 350 74102	Potentiometer 220E Lin
5B	9333 184 80112	Led SR103D
6B	4322 020 97070	Ferritring
7B	5722 660 20880	Mains connector
8B	3102 264 02020	Mask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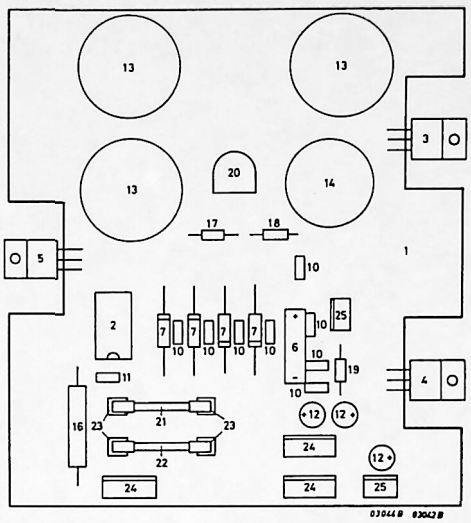
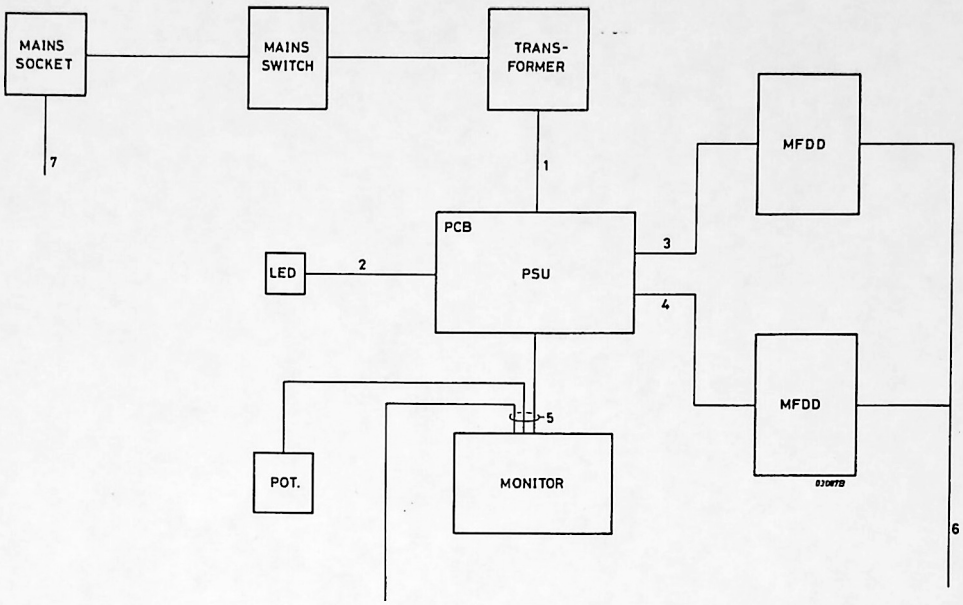
Pos.	Code Number	Description
B	5103 108 50810	Power Supply monitor compl.
1C	5103 107 53380	Cooling plate
2C	5103 107 53390	Bracket
3C	5103 108 50350	PCB power supply monitor compl.
4C	9390 261 90112	Spring clip
5C	5103 101 40950	Bracket
6C	5103 108 71720	Connector 4 pins


13
13
13
14
20
3
5
17
18
1
10
2
7
10
6
25
19
11
16
23
21
22
12
24
25

Pos.	Code Number	Description
1C	5103 108 50350	PCB power supply monitor compl.
2D	9332 955 50112	IC µA723A
3D	9332 996 00112	Voltage regulator 7805CU
4D	8203 235 09220	Voltage regulator LM340T12
5D	9332 699 50112	Transistor BD645
6D	9330 873 30112	Rectifier BY164
7D	9332 116 80682	Diode 1N5401
10D	2222 629 01103	Capacitor 10nF 63V
11D	2222 630 01272	Capacitor 2nF7 100V
12D	2012 017 01015	Capacitor 10µF 35V
13D	2222 033 47332	Capacitor 3300µF 40V
14D	2222 033 45472	Capacitor 4700µF 16V
16D	2306 330 03157	Resistor 0E15 5W
17D	2322 211 23822	Resistor 8K2
18D	2322 211 23123	Resistor 12K
19D	2322 211 23271	Resistor 270E
20D	2322 482 20472	Trim potentiometer 5K
21D	2422 086 01034	Fuse 4A
22D	2422 086 01031	Fuse T 2A
23D	5103 101 00020	Fuse holder
24D	2422 025 03345	Connector 5 poles
25D	2422 025 03343	Connector 3 poles


MAINS SOCKET
MAINS SWITCH
TRANS-FORMER
MFDD
7
1
PCB
PSU
LED
2
3
4
MFDD
5
POT.
MONITOR
6

Pos.	Code Number	Description
1	5103 107 80540	From transformer to PCB PSU
2	5103 107 80550	From PCB PSU to Led
3	5103 107 80490	From PCB PSU to MFDD (long)
4	5103 107 80500	From PCB PSU to MFDD (short)
5	5103 107 80420	From PCB PSU to, monitor, pot. meter
6	5103 107 80390	From MFDD to cabinet
7	5722 660 22320	Mains cable (English)
	5722 660 30670	Mains cable (European)

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2012 572 10011	5322 122 34238	CAP. 100N 63V
2013 017 01007	5322 124 14075	CAP 1UF
2013 017 01012	5322 124 14064	ELCO 4MU7 35V
2013 017 01015	5322 124 14033	ELCO 10MU 35V
2013 017 01022	5322 124 14052	ELCO 3M3 16V
2013 017 01031	5322 124 14183	ELCO 33MU 16V
2013 017 01107	5322 124 14184	ELCO 15MU 35V
2013 017 01157	5322 124 14185	ELCO 47MU 10V
203A3502103M1	5322 124 10322	
2122 118 00193	5322 111 94244	4310R-101-151
2122 118 00199	5322 111 94245	4308R-101-683 BOURNS
2222 017 16471	4822 124 20784	ELCO 470MU 25V
2222 033 45682	4822 124 20783	ELCO 6800MU 16V
2222 033 46332	4822 124 20789	ELCO 3300MU 25V
2222 629 01103	4822 122 30043	CAP. 10NF 63V
2222 630 03471	4822 122 31177	CAP. 470PF 100V
2222 641 10101	4822 122 31081	CAP. 100P 100V
2222 641 10279	4822 122 30045	CAP. 27P 100V
2222 641 10339	4822 122 31067	CAP. 33P 100V
2222 641 10479	4822 122 31072	CAP. 47P 63V
2222 641 52399	4822 122 31069	CAP. 39PF 100V
2222 642 10229	4822 122 31063	CAP. 22P 100V
2222 642 10689	4822 122 31349	CAP. 68P 100V
2222 808 11279	4822 125 50088	TRIM-CAP.FOIL 2/30PF
2322 211 23102	4822 110 73107	RES. 1K0 CR25
2322 211 23121	4822 110 73083	RES. 120E CR25
2322 211 23124	4822 110 73163	RES.1120K CR2 5
2322 211 23153	4822 110 73138	RES. 25K CR25
2322 211 23181	4822 110 73087	RES. 180E CR25
2322 211 23183	4822 110 73141	RES. 18K CR25
2322 211 23221	4822 110 73089	RES. 220E CR25
2322 211 23222	4822 110 73116	RES. 2K2 CR25
2322 211 23271	4822 110 73092	RES.270E CR25
2322 211 23273	4822 110 73145	RES. 27K CR25
2322 211 23331	4822 110 73094	RES. 330E CR25
2322 211 23332	4822 110 73121	RES. 3K3 CR25
2322 211 23361	4822 110 70095	RES. 360E CR25
2322 211 23391	4822 110 73096	RES. 390E CR25
2322 211 23393	4822 110 73149	RES. 39K CR25
2322 211 23471	4822 110 73098	RES.470E CR25
2322 211 23472	4822 110 73125	RES. 4K7 CR25
2322 211 23473	4822 110 73152	RES. 47J CR25
2322 211 23561	4822 110 73101	RES. 560E CR25
2322 211 23562	4822 110 73127	RES. 5K6 CR25
2322 211 23563	4822 110 73154	RES. 56K CR25
2322 211 23684	4822 110 73183	RES. 680K CR25
2322 211 23689	4822 110 73076	RES. 68E CR25
2322 350 74102	4822 101 20293	POTM. 220E LIN
2322 409 47261	5322 101 14288	RES.100K 0,2W 20%
2413 535 00322	5322 157 54178	COIL 100MUH
2422 025 01899	5322 265 54068	CONNECTOR 20POL.
2422 086 00033	4822 253 20018	FUSE 1A
2422 086 00049	4822 253 20027	FUSE 5A
2522 163 54007	4822 502 30188	PAN-TAPSCREW 2,9X9,5
3103 200 57300	5322 209 14717	IC Z80-CTC ZILOG
3103 200 57620	5322 209 14716	IC Z80-CPU ZILOG
3103 200 57740	5322 111 94246	4310R-101-472 BOURNS
3103 209 11670	4822 276 10483	MAINS SWITCH
3103 220 40610	4822 401 10632	CABLE STRAP
3103 221 05370	5322 492 64762	CONTACT SPRING

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
3103 238 73250	5322 255 44171	IC-SOCKET 24POL.
3103 238 73260	5322 255 44047	IC-SOCKET 28POL.
3103 238 73270	5322 255 44217	IC.SOCKET 40POL.
3112 318 37190	5322 146 24481	MAINS TRAFO TS524
3112 318 37280	5322 146 24482	TRAFO TG538
3119 208 54860	5322 214 45347	PRINTED BOARD MAIN
3119 208 54870	5322 214 45348	PRINTED BOARD VIDEOO
3119 208 54880	5322 150 14049	DEFLECTION UNIT
3122 111 90060	4822 492 61974	SPRING
4322 143 04040	4822 242 70323	X-TAL 4,433619 MHZ
5103 101 00020	4822 256 30171	FUSE HOLDER
5103 101 40810	5322 414 26405	PUSH-ON FIX
5103 104 00230	5322 414 34263	TURNING KNOB (FRONT)
5103 104 12120	5322 414 26406	KNOB
5103 104 12210	5322 414 34264	ADJUSTING NUT
5103 107 53010	5322 218 74547	MONITOR 12" CPL.
5103 107 53060	5322 447 94644	COVER MFD
5103 108 00470	5322 216 25635	PCB NETZTEIL
5103 108 00500	5322 216 25637	PCB CPU (BUSINESS)
5103 108 00520	5322 216 25639	PCB EXTENSION
5103 108 00540	5322 216 25641	MODULATOR UNIT CPL
5103 108 01210	5322 216 25636	PCB CPU (ECONOMY)
5103 108 01220	5322 216 25638	PCB VIDEO
5103 108 20130	5322 156 24282	COIL
5103 108 50880	5322 397 34018	TEST ROM CASSETTE
5103 108 70200	5322 255 44107	IC MOUNTING
5103 108 70220	5322 255 44112	IC-SOCKET 18POL.
5103 108 70670	5322 280 14028	CER.RESONATOR
5112 291 42910	5322 278 14005	SWITCH
5112 291 43290	5322 278 14006	KEY-SWITCH
9300 804 80000	5322 131 24091	PICTURE TUBE M31-333
9330 839 90112	4822 130 30621	DIODE 1N4148
9330 873 30112	4822 130 30414	DIODE BY164
9331 176 90112	5322 130 34916	DIODE BZX79C3V9
9331 492 00112	4822 130 40855	TRANSISTOR BC337
9331 976 40112	4822 130 40938	TOR BC548
9331 977 30112	4822 130 40941	TOR BC558
9332 014 50112	5322 209 84035	IC N7416N
9332 116 80112	5322 130 34939	RECTIFIER 1N5401
9332 243 90112	5322 209 85824	IC SE555N
9332 414 60112	5322 209 84285	IC N7438N
9332 642 80112	5322 130 44786	TOR BD675
9332 776 10112	5322 209 10002	IC CD4029 BF
9332 825 80112	5322 209 14433	IC HEF40097BP
9332 826 10112	5322 209 84508	IC HEF4022BP
9332 830 60112	5322 209 86327	IC 705MIN7406A
9332 864 20112	5322 209 84515	IC N7414N
9332 865 80112	5322 209 84023	IC N74107N
9332 869 00112	5322 209 84823	IC N74LS00A
9332 869 20112	5322 209 85265	IC SN74LS03N-00
9332 869 30112	4822 209 80621	IC N74LS04A
9332 869 50112	5322 209 84995	IC SN74LS08N-00
9332 869 70112	5322 209 84996	IC N74LS10A
9332 869 80112	5322 209 85604	IC N74LS11A
9332 869 90112	5322 209 85504	IC N74LS12A
9332 870 70112	5322 209 85561	IC N74LS27A
9332 870 90112	5322 209 85311	IC N74LS32A
9332 871 10112	5322 209 85605	IC N74LS38A
9332 872 20112	5322 209 84997	IC SN74LS86N-00
9332 872 90112	5322 209 85974	IC SN74LS109AN

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
9332 873 40112	5322 209 85201	IC SN74LS132N
9332 873 50112	5322 209 85647	IC N74LS138B
9332 873 60112	5322 209 85839	IC N74LS139N
9332 873 70112	5322 209 86276	IC N74LS145B
9332 873 90112	5322 209 85488	IC N74LS153B
-		
9332 874 00112	5322 209 85489	IC N74LS157B
9332 874 80112	4822 209 80779	IC N74LS174B
9332 874 90112	5322 209 84999	IC SN74LS175N-00
9332 875 40112	5322 209 85405	IC N74LS193N
9332 876 60112	5322 209 86016	IC N74LS293N
-		
9332 886 70112	5322 209 85312	IC N74LS02A
9332 912 00682	5322 209 84308	IC MC1489L
9332 963 20682	5322 209 84307	IC MC1488L
9332 972 60112	5322 209 85615	IC N74LS85N
9332 996 00112	5322 209 84841	VOLT.REG. 7805CU
-		
9333 184 80112	4822 130 30926	LED SR103D
9333 201 80112	4822 130 31273	DIODE OF420
9333 203 30112	4822 130 30924	LED LD30/1
9334 121 80112	5322 209 85792	IC N74LS273N
9334 247 50682	5322 209 14856	IC MK4116-4
-		
9334 286 70112	4822 209 10047	IC SAA5020
9334 287 00112	4822 209 10046	IC SAA5050 (UK+NL)
9334 294 50682	5322 209 54663	RAM HM.472114/4
9334 452 00682	5322 209 86431	IC INT3216
9334 452 40682	5322 209 86432	IC DM81LS97
-		
9334 494 30112	4822 209 80546	IC SAA5052 (S)
9334 510 30112	5322 209 85915	IC SN74LS161AN
9334 510 40112	5322 209 85863	IC N74LS163AN
9334 617 20112	4822 209 80782	IC N74LS74A
9334 682 90112	5322 209 14424	IC MK1007P
-		
9334 908 00682	5322 209 86433	IC DP8304
9335 036 70112	4822 209 80593	IC SAA5051 (G+A)
9335 043 40112	5322 209 85558	IC SN74LS367
9335 183 20682	5322 209 86434	IC LM79L05
9335 183 30682	5322 209 86435	IC LM79L12
-		
9335 203 40682	5322 209 86436	IC LM1886
9335 203 50682	5322 209 86437	IC LM1889
9335 284 70682	5322 209 86438	IC PD765
9390 261 80112	4822 255 40179	SPRING CLIP 56363
9390 261 90112	4822 492 62242	SPRING CLIP 56364
-		
9390 264 10112	4822 255 40181	MICA INSULATOR 56369

END OF REPORT

7 TROUBLESHOOTING AND REPAIR

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7 TROUBLESHOOTING AND REPAIR

7.1 MAINTENANCE PROGRAM

The program provides means to test the functional correctness of the P2000 microcomputer. After inserting the command module and depressing the RESET button the NATIONAL VERSION SELECTION MENU appears on the screen. The operator must type the number that corresponds tot the national version of his machine, i.e. 1 for German, 2 for French, 3 for English or Dutch and 4 for swedish. The selected national version is considered at the handling of keyboard, screen and printer, but THE MESSAGE AND DISPLAYED IS ENGLISH IN ALL NATIONAL VERSIONS.

Next follows the MAIN SELECTION MENU, where the operator can select the test he wants to do. Each test is realized as a separate module. The test modules are: MEMORY, PRINTER, KEYBOARD, SCREEN, TAPE, BEEPER and DISK. Auxiliary modules are the PROTOCOL and the DEBUGGER.

Some testing modules are divided into submodule. They can be reached through separate menus. By typing ZERO the user can return to the main selection menu. The testing results are displayed as well as printed. If the printer is not connected, message is sent (the only exception is the printer test).

7.1.1 MEMORY TEST

After selecting '1' in the main selection menu (or if the basic RAM is defect after RESET) the memory is tested as follows. The first location (5000) is written by a random byte and in the following pattern the data on the next address is computed from the previous one by adding constant (53H) and the high and low address of that byte.

Then this pattern is 'disturbed' by

1. writing 00H to all port addresses
2. fast moving of the Video RAM range one line forward.

After restoring of Video RAM range follows the actual testing procedure separately for each range. The ranges are:

1. 5000 57FF Video RAM
2. 5800 5FFF Video RAM second range (only in the professional version)
3. 6000 9FFF Basic RAM
4. A000 DFFF Extension RAM first range
5. E000 FFFF Extension RAM second range (sw bit = 0)
6. E000 FFFF Extension RAM second range (sw bit = 1)

At first the 0 byte of the ranges checked for correctness, than each bit is inverted twice. After each writing operation follows a reading and testing one. To each range corresponds one CPU register. In case of any erroneous bit the corresponding register bit is set. If all the 8 bits in this range are set, the test of that range is terminated, thus saving testing time.

When this test is ready for all the bytes or the ranges each bit is inverted one by one (and tested of course), i.e. all bytes of the range are inverted.

This procedure is repeated for all ranges and afterwards repeated once again for the whole memory range.

This result has the following format:

```
5000 - 57FF
5800 - 5FFF
6000 - 9FFF
A000 - DFFF       BAD BITS: 1 3 6
E000 - FFFF (1)
E000 - FFFF (2)   NOT AVAILABLE
```

In the ranges without remark no error has been found. The 'BAD BITS' remark means that at least one error has been found on the bit positions mentioned. Ranges with 'NOT AVAILABLE' are either missing completely or error bas been found on all the eight bit positions. To obtain a more detailed information about the behaviour of the memory the operator can enter the DEBUGGER.

When the result is displayed and printed, the beeper sounds and a waiting loop is started. Its length is 30 sec if 'BAD BITS' have been found, otherwise 15 sec. If any error has been found, the beeper sounding all the time. (It is not an error when the second page of the video RAM is missing rather the normal case at the 'economy' version). During the waiting loop the keyboard is checked. If no key is depressed, the memory test repeated with another pattern. Otherwise the NATIONAL VERSION SELECTION MENU appears again (because the memory test has deleted the corresponding information).

7.1.2 PRINTER TEST

Two submodules of the printer can be selected by a menu:

1. Printer character test
2. Socket static test

Printer character test gives a general information about the computer - printer communication. It is very imporant that the COMPUTER SHOULD BE PREPARED FOR THE KIND OF PRINTER THAT IS USED (matrix or daisy wheel). In doubt choose PROTOCOL in the main selection menu and type RETURN.
If your printout is wrong, check the print-wheel (on daisy-wheel printer) or the national version setting (on the matrix printer) or national version setting (on the matrix printer). It is also possible that some other MICRO SWITCHES on the printer are incorrect. A new switch position is acknowledge any AFTER SWITCHING THE PRINTER OFF AND ON.

If no printout is obtained and the printer cable is also perfect, use SOCKET STATIC TEST. It gives information about the static behaviour of the input and output ports. Follow the instructions appearing on the screen, i.e. at first REMOVE any connector from the socket, then CONNECT the required pins with a wire and type 'Y' if ready. Then resulting table shows the errors. The correct result can be seen in the next table. It should be noted that the input pin-2 is not involved in the printing procedure, and an error here does not prevent printing.

	OUTPUT	INPUT		0 = -12V
PIN	03	02	20	1 = +12V
EMPTY CONNECTOR	1	1	1	
CONNECT 03 02	0	0	1	
	1	1	1	
CONNECT 03 20	0	1	0	
	1	1	1	

7.1.3 KEYBOARD TEST

The keyboard is displayed on the screen and at first all positions are inverted (professional version) or coloured with magenta (economy version). The keys must be depressed ONE BY ONE beginning in the left upper corner and going to right. If the first line is ready, the second must be started with the leftmost key etc. If a key is accepted, the corresponding position becomes non-inverted (professional v.) or green (economy v.). If the key sequence is incorrect i.e. not the expected key is depressed, the beeper sounds. If some keys are NOT ACCEPTED and no key is depressed WITHIN 5 SECONDS, a question appears: CONTINUE (Y/N). If the answer is Y, the test can be continued, otherwise the figure of the keyboard test is printed. In this figure ALL DEPRESSED KEYS are marked with '=' the bad ones with the a symbol characteristic to that key (or '*').

7.1.4 SCREEN TESTS

7.1.4.1 SCREEN CHARACTER TEST

The aim of this test is to check whether the character generator displays all screen codes correctly.

At first appears an explaining text on the screen. After typing RETURN follows the first picture. It contains 23 lines each with the same characters. The correct sequence of them is shown in Appendix-D. The cursor is set to the beginning of the first line. The operator should observe the characters and decide whether they are correct. If the page is OK, the answer is TAB or RETURN. Otherwise the cursor should be positioned to the line with the rejected character by using the CURSOR UP or CURSOR DOWN keys and the DEFINE key should be depressed (shift and zero on the numeric pad). If all errors are marked, TAB or RETURN brings the next picture. This procedure is repeated until the message 'NO MORE CHARACTERS' appears. Above this line no empty line may appear, it is an error too. If any error has been marked, the hexadecimal screen codes of these characters are printed.

7.1.4.2 GRAPHIC TEST

Two pictures are generated where all graphics characters occur twice. Both pictures are symmetric and the second picture is the inverse of the first one. They must be perfect and must not vibrate. The operator should qualify them.

7.1.4.3 NATIONAL VERSION TEST

The aim of this test is to make sure that the national version of both the KEYBOARD and the SCREEN character generator agrees with the version entered in the NATIONAL VERSION SELECTION MENU. At first a character is displayed on the screen and the operator must type the corresponding key. If a wrong key is depressed, the beeper sounds and the operator can try it again. If the second and the third attempts are also wrong, the test is failed. If the proper key is depressed, two further characters must be found on the keyboard.

7.1.4.4 SCREEN ADJUST TEST

```
00000000000000000000000
0+++++++++++++++++++++0
0+++++++++++++++++++++0
0+++++++++++++++++++++0
0+++++++++++++++++++++0
00000000000000000000000
```

A similar picture is displayed as shown above to check that its LIMITS are properly adjusted on the screen. It is also important that the letters on the rands must have the WIDTH. The FOCUSING can be checked too. The operator should qualify the picture.

7.1.4.5 SPECIAL SCREEN TEST

In the professional version three lines are displayed to check the UNDERLINE, FLASH and INVERT features of the screen. Each second character must show the required feature. The operator should qualify the picture.
In the economy version at first a picture is shown with the required TV-screen features (ALPHANUMERIC and GRAPHICS in all different COLOURS, FLASH, DOUBLE HEIGHT, CONCEAL DISPLAY, NEW BACKGROUND, SEPARATE AND CONTIGUOUS GRAPHICS). When the operator has qualified the picture, a scroll test is performed, where the picture is moved right to left and then back again until a key is depressed. It it is Y or N, the feature is qualified and the test is ready. Otherwise the scrolling stops and on the next key it starts again.

7.1.5 TAPE DRIVE TEST

There are 2 static and 4 dynamic tests selectable. Before entering a dynamic test the tape must be in position, otherwise the program returns to the menu immediately.

7.1.5.1 TAPE STATUS TEST

This test is used to check the 'TAPE IN POSITION' and 'WRITE PROTECT' switches. The operator should follow the instructions on the screen (remove tape, insert write protected tape, insert write enabled tape) and each time type Y if ready. If error is found, the bad switch is displayed.

7.1.5.2 READ MASTER TAPE

To make sure that your tape unit reads properly use the master test tape produced of a known good machine. At first the tape is rewound and the header of the first record is evaluated. If it is not a MASTER or QUASI-MASTER tape or not write-protected, an error message is displayed together with the question 'CONTINUE (Y/N)'. If the answer is 'N', the test is aborted, otherwise continued. After the header-record follow the test data records. One record is 256 bytes long and has the following structure.

The first byte is the record number (1, 2, 3, ... for the first, second, third etc. records) and the following byte is by 3 higher than the previous one. The 'increment by 3' algorythm is continued till the end of the record.

If error is found, it is displayed and asked if continue. The master tape has 10 data records. If all have been tested or the test is aborted, the test result is sent to the printer.

7.1.5.3 WRITE, SKIP-BACK, READ TEST TAPE

This test checks the quality of the tape and the tape driver as well. The test tape must be write enabled (insert plug into the left-side hole). At the first is rewound, then a record with the 'test header' is written, rewound and read again. Then follows the first data record. If everything is OK, the message '01. RECORD OK OK OK' appears, showing the results of the write, skip-backward and read operations. Then follows the next record and the message is over-written. In case of error the message is displayed and asked if continue. In case of NO MARK error the test can not be continued: a serious is happened. The procedure is repeated until the end of tape (cca 40 records). The user can cancel the testing by opening the door of the tape driver, then the NOT READY message is displayed.

7.1.5.4 CONTINUOUS WRITE, SKIP-BACK, READ TEST

At first the operator must be decide either for full print (with OK messages) or for partial print (only with error messages).
This test performs the same procedure as the previous one (5.3), with the differences:

1. In case of error the test carries on without operator's action.
2. When the tape is full, it rewound and the test is continued at the beginning. To disrupt the test the door of the tape drive must be opened.

7.1.5.5 CREATE QUASI-MASTER TAPE

As a matter of fact, this is an auxiliary procedure, not a testing one. You can create here the pattern of the master tape with the restrictions described in 5.2. The procedure run similarly as in 5.3.

7.1.5.6 CONTINUOUS STATUS TEST

This is an auxiliary procedure for the adjusting of the TAPE IN DRIVE and the WRITE PROTECT switches. If you insert a tape, you can see continuously the status of these bits and adjust exactly the switching points.

7.1.6 BEEPER TEST

The beeper is activated and the user must decide whether it is OK or not. An incorrect answer (neither Y not N) results in the repeated beeper sound and you can repeat it several times.

7.1.7 DISK DRIVE TESTS

The disk testing procedures test the disk and the drive at the same time therefore if an error is found, it can be the error of the disk too.

7.1.7.1 READ MASTER DISK

To make sure that your disk drives read properly use the MASTER TEST DISK delivered by PHILIPS. If you do not have such a disk, you can create the master pattern by the WRITE-READ TEST DISK procedure. It does not guarantee, however, that your computer can read without error the disks written on other P2000 machines.

At first the question 'DRIVE 1 READY (Y/N)' is displayed. If you want to test only drive-2 your answer is 'N', otherwise 'Y'. The disk should be inserted previously in the corresponding drive (1 is left, 2 is right). The master disk must be WRITE PROTECTED (the write protection notch must be covered by a label).

Then the head is moved to TRACK-34 and the identifier is read to check the track number. Afterwards a step is made to TRACK-0 thus testing the stepping function. Now follows the actual reading test. Each track is read and tested for the master pattern (first byte is the track number, the next byte is incremented by 3 etc.). If ERROR IS FOUND, THE OPERATION IS REPEATED UP TO 7 TIMES. Then the operator should decide whether it is continued or not. If the disk is properly written, but NOT CONTAIN THE MASTER PATTERN, the error message is WRONG DATA. A detailed description of error messages is given in Appendix-F.
After reading of track-34 the question 'DRIVE 2 READY ' is displayed and the user can start or cancel the testing of drive-2 by answering Y or N.

7.1.7.2 WRITE-READ TEST DISK

A formatted diskette should be inserted in the drive under test. The drive selection is performed the same way as by 'Read master disk'. The disk is written with the MASTER PATTERN starting with track-0 to track-34. Then the tracks are read and compared with the master pattern from track-34 to track-0.

7.1.7.3 CONTINUOUS WRITE TEST DISK

The user can define which drive should be tested (1,2 or both). The procedure is the similar to 7.2 with the following differences:

1. In case of error no operator action is required.
2. If the test is ready, it is repeated unlimited. The PASS number shows the number of repetitions. The test can be disrupted by opening the door of the drive under test.

7.1.8 PROTOCOL

This auxiliary module gives a summary of the machine properties. It has the following format:

```
SERIAL NUMBER: 1 2 3 4 5 6 7 8 9 0
NATIONAL VERS: UK
TYPE:          PROFESSIONAL 48K USER RAM
PREPARED FOR:  DAISY-WHEEL PRINTER
DATE           23-10-1980
INSPECTED BY:  Abcdefghijk Lmnopqrstuvwx
```

The serial number must be type by the user (up to 20 characters) or omitted simply by typing RETURN. THe NATIONAL VERSION is taken from the national version selection menu. The TYPE can be professional (if the Auxiliary Video range 5800-5FFF is present) or economy (if not). The user RAM can be 16, 32 or 48k.
The machine can prepared either for daisy-wheel or for matrix printer. The date and the name of the inspector is typed by the user (or omitted by RETURN).

7.1.9 DEBUGGER

This auxiliary module has the following features.

- display and modify memory
- Read, modify and write tape data

It is very useful to study the memory behaviour in case or error and to check and repair data on tape.

The debugger has the 12 commands. The numbers used in the commands are always HEXADECIMAL. The command lines must be terminated by RETURN. To correct a wrong entry the BACKSPACE and DELETE LINE keys can be used. The debugger uses the user RAM range 6100-61FF. Writing in this range may lead to irregular results. The following commands are implemented.

C: Compares the contents of two memory blocks. Example: C 7000 8000 280 (C addr-1 addr-2 length). The memory blocks 7000-727F and 8000-827F are compared and differing bytes are displayed.

D: Display or change memory. Example-1:
D 9210 140 (D address length)
The contents of the range 9210-934F is displayed.

Example-2:
D 8840 (D address)
8840 28
At first the Debugger displays the contents on the given location. The answer can be:

1. An other hexadecimal byte to change the byte.
2. RETURN to ask for the next byte.
3. Q to leave the change mode.

F: Fill memory with data. Example:
F7100 2B0 3F (F start-addr length)
The range 7100-73AF is filled with 3F.

M: Move memory block. Example:
M6400 7C00 2B0 (M destination source length)
The range 7C00-7AF is copied into the range 6400 66AF.

P: Reads ana/or writes ports. Example-1:
P and RETURN reads all ports 0 to FF. In the professional version this command results in screen disturbances. It can be overcome by writing 0 to Port-7F.

Example-2:
P 3F
3F 9C Reads and displays the data from Port-3F. The answer can be:

1. An other hexadecimal byte to write on the port.
2. RETURN to ask for the next port address.
3. Q to leave change mode.

Q: Leaves the debugger and returns to the main selection menu.

S: Search string. Example:
S 21 00 50 ... (up to 5 bytes) searches this string in the whole memory and displays the adresses where it occures.

TI: Tape initialize (rewind).
TF: Tape forward 1 block (1 block = 1K = 400 Hexadecimal)
TB: Tape backward 1 block

TR: Tape read. Example:
TR 8000 800 (TR address length) reads 2 blocks from the tape and stores the data in the 8000-87FF range.

TW: Tape write. Example:
TW 9000 C00 (TW address length) writes 3 blocks onto the tape from the 9000 9BFF range.